REVIEW PROBLEMS FOR THE FINAL

I. Introduction

1. There are a total of 14 problems in this review handout. Problems 1 through 3 serve as review of basic material. The final exam is going to concentrate on problems 4 through 14. Some information about the exam:

i. The exam is on Saturday, December 18th 2004, from 8:00 AM to 11:00 AM in 234 Hearst Gym.

ii. You may use a calculator.

iii. The exam has 5 questions. They each have different parts. The important concepts covered on each question are:

   1. Op-amp analysis
   2. Oscillators
   3. Flip-flops
   4. Op-amp frequency analysis
   5. Diode Driving-point characteristics

Understanding the concepts in these review problems should help you do really well on the exam. Please do not waste time trying to memorize these problems – that is not going to help you on the final. **You should also understand the flip-flop problem (question 5) in homework 9 (PLEASE DO THIS, I DO NOT HAVE A FLIP-FLOP PROBLEM IN THIS REVIEW PACKET) and the driving point characteristic problem in homework 7 (problem 3). The solutions are available in 140AB Cory (the EE100 lab). You may browse them anytime a TA is in there – BUT, do NOT take them out of the lab. Finally, UNDERSTAND section 9.6 in the book (pp. 495 – 499), this will help with problem 5 on the final exam.**

2. There is a review session scheduled on Saturday, December 11th 2004, 9:00 AM – 11:00 AM, location: TBA. I will try to answer any questions you have on these review problems and other material from class. I will hand out solutions to these review problems.

3. Here are my extra office hours for the final: Thursday (12/16): 6:00 pm – 12:00 AM (midnight), Friday (12/17): 3:00 pm – 9:00 pm. All office hours are going to be held in the Free Speech Cafe next to the Moffit library since Cory hall is a pain in the a** to get in after-hours. 204B Cory (the location of my Sunday office hours) is unavailable during those days. I DO NOT have office hours on Sunday and Wednesday anymore.

IN CONCLUSION, ON THE FINAL: READ THE QUESTION, THINK, THEN ANSWER!

Ref.: 1. Nilsson and Riedel, *Electric Circuits*, 6th Edition, McGraw-Hill.
2. Chua, Desoer and Kuh. *Linear and Nonlinear Circuits*. McGraw-Hill.

(1) Figure 1 below shows a model for the MOS transistor. Using this model in the circuit below, find v_0 and V_{DS}.

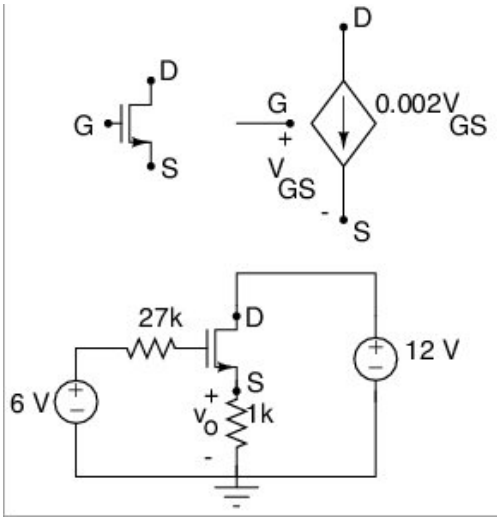


Figure 1. Transistor model and circuit for problem 1

(2) Find the equivalent resistance as seen at terminals ab in the circuit in figure 2.

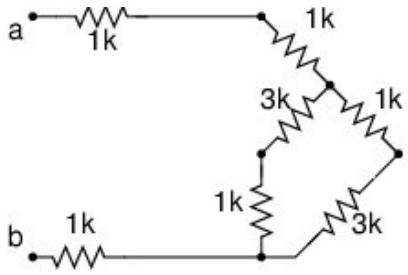


Figure 2. Circuit for problem 2

(3) Find the thevenin equivalent at terminals ab in the circuit below.

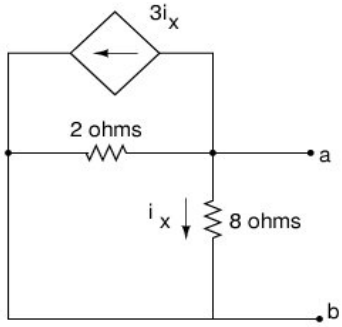


Figure 3. Circuit for problem 3

(4) In the figure 4 (a), assume the open loop gain of the op-amp is really big (say 10^6). Assume E_{sat} = 12 V.

i. Sketch the transfer characteristic when E = 5 V.

ii. Sketch the transfer characteristic when E = -5 V.

iii. Sketch $v_o(t)$ for the $v_{in}(t)$ shown in figure 4 (b). ASSUME: E = 0 V and the maximum and minimum value of v_{in} is 5 V and -5 V respectively.

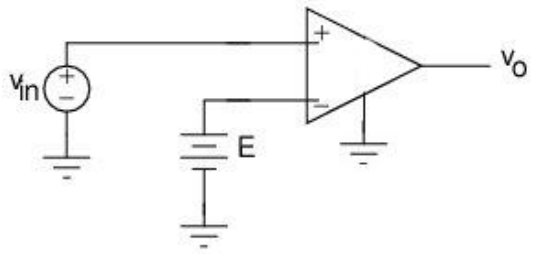


Figure 4 (a). The comparator

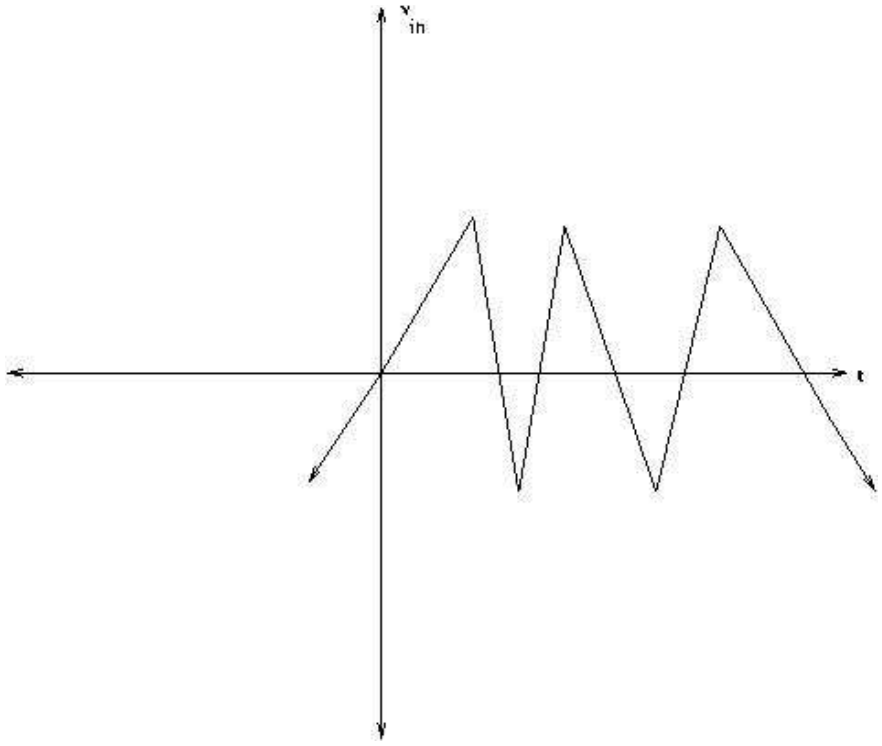


Figure 4 (b). Sample input voltage for figure 4 (a).

(5) Find v_o as a function of v1 and v2 in the circuit below. Assume op-amp is operating in the linear region.

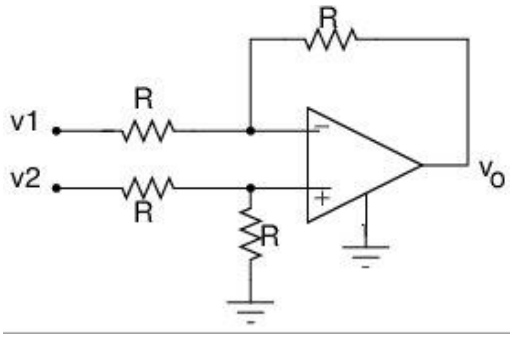


Figure 5. Circuit for problem 5.

(6) In the circuit in figure 6, find $\frac{\mathbf{v_o(jw)}}{\mathbf{v_i(jw)}}$. Assume op-amp is operating in the linear region. Give your answer in the form $\frac{\mathbf{a+jb}}{\mathbf{c+jd}} = \mathbf{H(jw)}$.

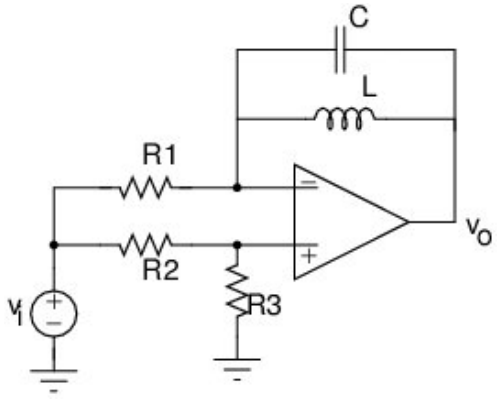


Figure 6. Circuit for problem 6.

(7) In the circuit in figure 7, find $\frac{\mathbf{v_o(jw)}}{\mathbf{v_i(jw)}}$. Assume op-amp is operating in the linear region. Give your answer in the form $\frac{\mathbf{a+jb}}{\mathbf{c+jd}} = \mathbf{H(jw)}$.

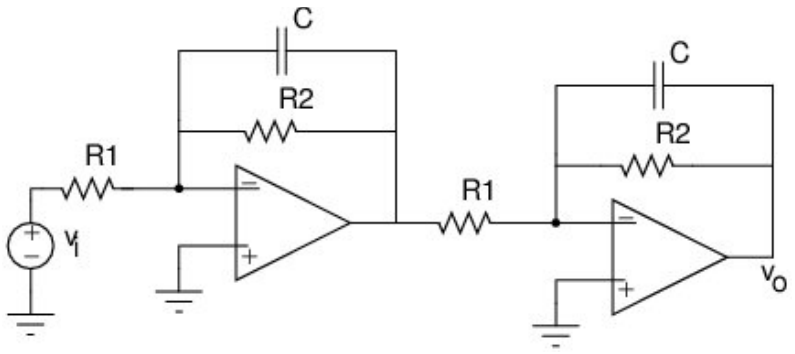


Figure 7. Circuit for problem 7.

(8) Consider the circuit shown in figure P6.20 (a) where N is described by the i-v characteristic shown in figure P6.20 (b).

i. Indicate the dynamic-route. Label all equilibrium points and state whether they are stable or unstable.

ii. Suppose $v_c(0) = 15$ V. Find and sketch $v_c(t)$ and $i_c(t)$ for $\mathbf{t} \geq 0$. Indicate all pertinent information on the sketches.

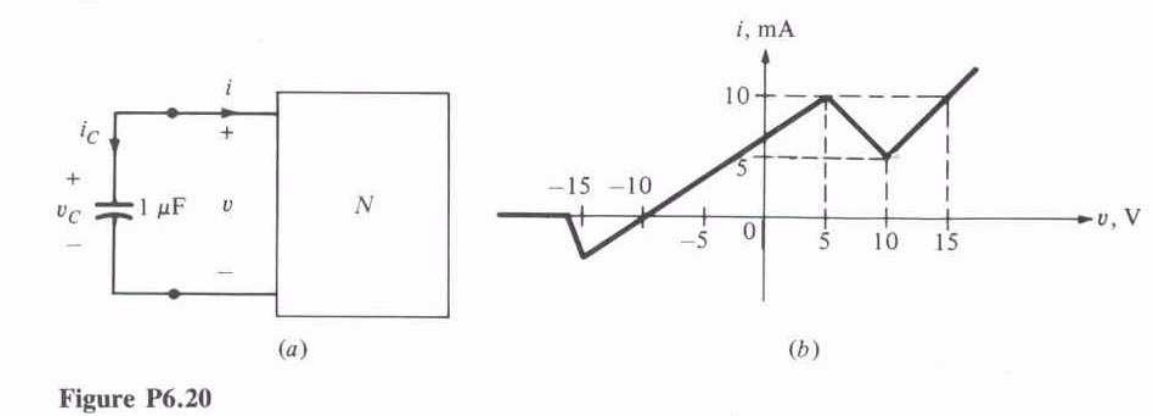


Figure P6.20

(9) Consider the circuit shown in figure P6.21 (a) where N is described by the i-v characteristic shown in figure P6.21 (b).

i. Indicate the dynamic route. Label all equilibrium points and state whether they are stable or unstable.

ii. Suppose $i_L(0) = -20$ mA; calculate and sketch i(t) and v(t) for $\mathbf{t} \geq 0$.

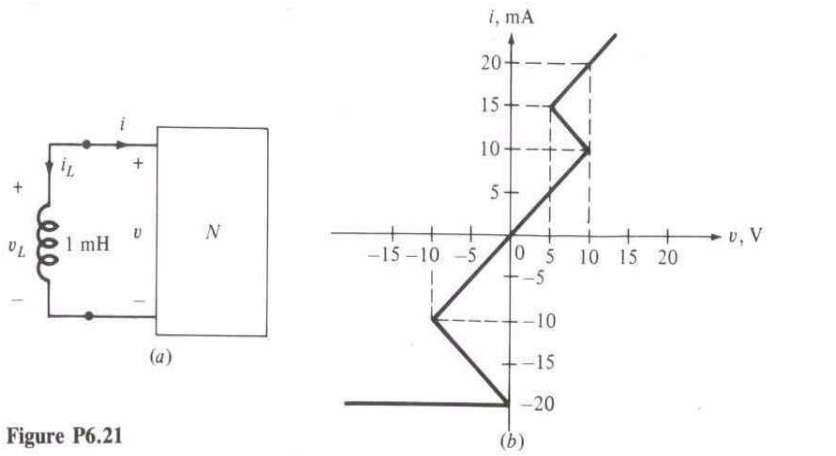


Figure P6.21

(10) For the circuit in figure P6.22 (a) with the nonlinear resistor i-v characteristic as shown in figure P6.22 (b), find all equilibrium states and classify each as stable or unstable:

i. when switch S is in position 1.

ii. when switch S is in position 2.

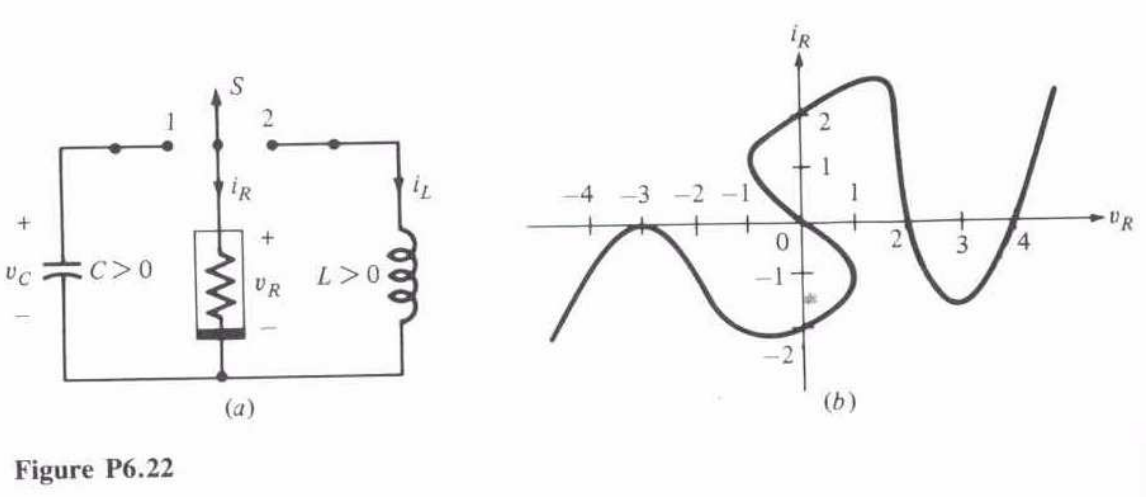


Figure P6.22

(11) Consider the circuit shown in figure P6.23 (a) where N is described by the i-v characteristic shown in figure P6.23 (b).

i. Sketch the dynamic route.

ii. If $v_c(0) = 2$ V and $i_c(0) = -2$ mA; calculate and sketch i(t) and v(t) for $\mathbf{t} \geq 0$.

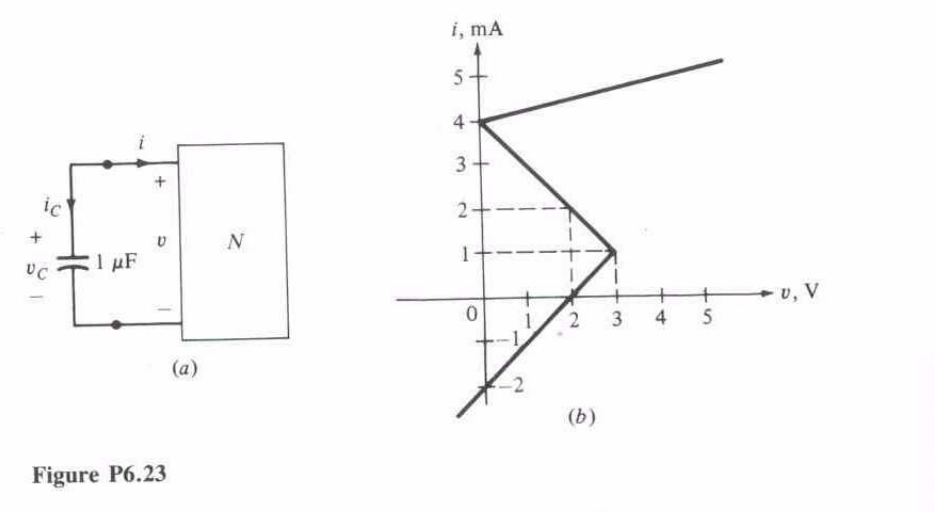


Figure P6.23

(12) Consider the circuit in figure P6.21 (a) along with the i-v characteristic shown in figure P6.24.

i. Sketch the dynamic route.

ii. For what range of initial condition $i_L(0)$ does this circuit exhibit oscillation?

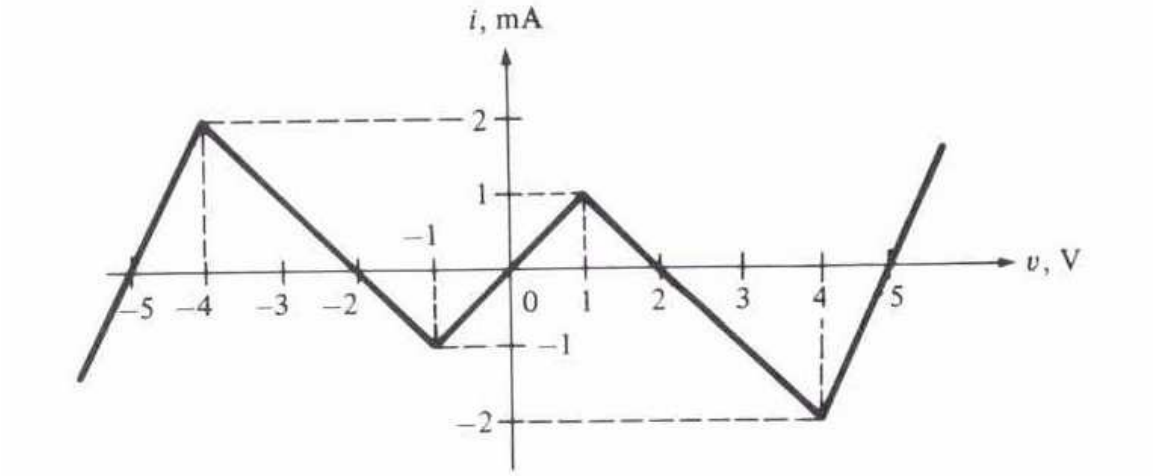


Figure P6.24

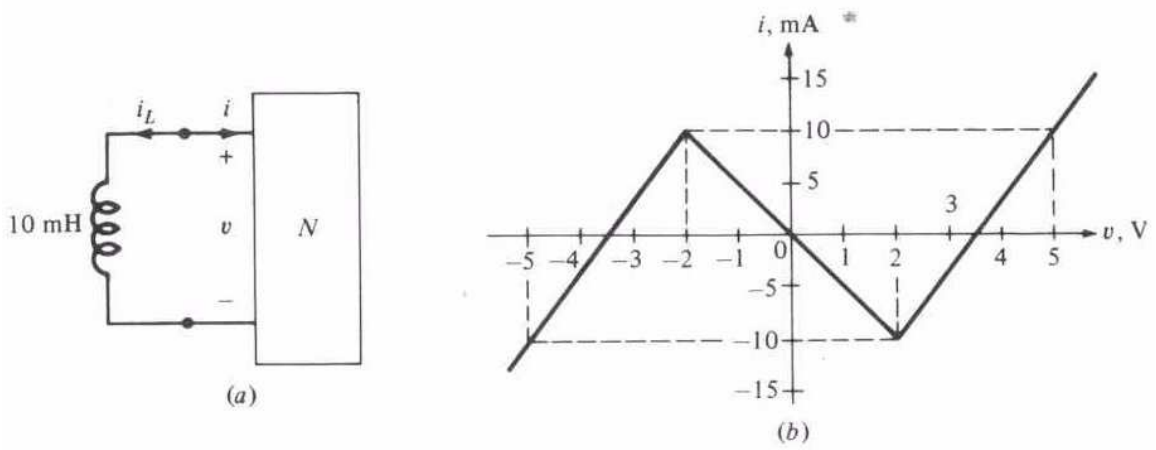
(13) Consider the circuit shown in figure P6.25 (a) where the one-port is described by the i-v characteristic in figure P6.25 (b).

i. Sketch the dynamic route.

ii. If $i_L(0) = -15$ mA, find and sketch i(t) and v(t) for $\mathbf{t} \geq 0$

iii. Determine all switching times.

iv. Calculate the period of oscillation.



(14) Plot the driving-point characteristics of the one-ports shown in figure P2.4. You can use graphic series and parallel addition or any other method of your choosing. Assume all diodes are ideal.

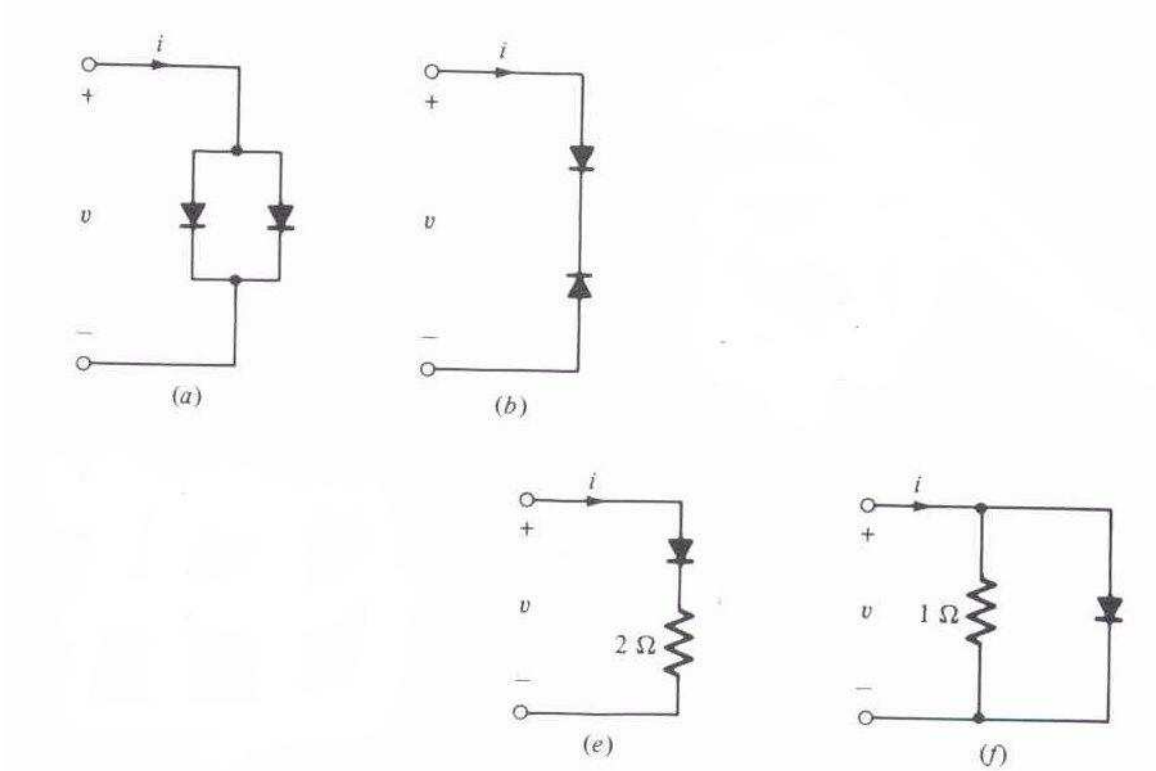


Figure P2.4