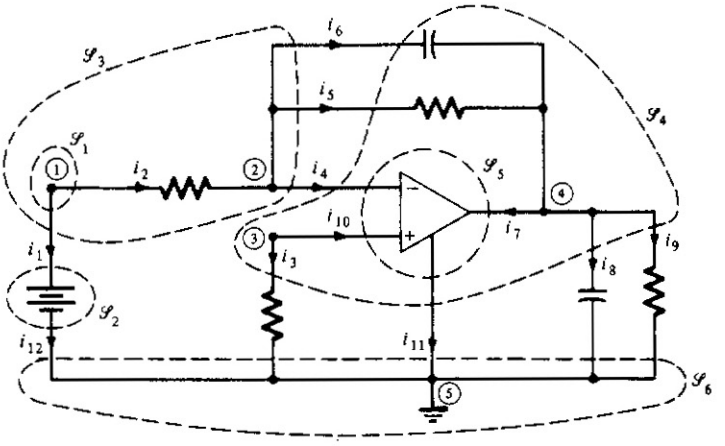

Figure 4.4 An op-amp circuit illustrating gaussian surfaces and KCL.

at nodes ②, ③, ④, and ⑤. The properties of the op amp will be treated in Chap. 4. In the figure we draw six gaussian surfaces: $\mathcal{S}_1, \mathcal{S}_2, \ldots, \mathcal{S}_6$. We will use these surfaces to illustrate Kirchhoff's current law:

> *KCL* For all lumped circuits, for all gaussian surfaces $\mathcal{S}$, for all times t, the algebraic sum of all the currents *leaving* the gaussian surface $\mathcal{S}$ at time t is equal to zero.

For $\mathcal{S}_1$, KCL states:

$$i_1(t) + i_2(t) = 0 \qquad \text{for all } t$$

Note that $\mathcal{S}_1$ contains only node ① in its "inside"; thus a node may be considered as a special case of a gaussian surface, i.e., the surface is shrunk to a point.

For $\mathcal{S}_2$, KCL states:

$$-i_1(t) + i_{12}(t) = 0 \qquad \text{or} \qquad i_1(t) = i_{12}(t)$$

Note that $\mathcal{S}_2$ encloses the two-terminal element, namely, the battery. Thus we make the conclusion that for a *two-terminal element*, the current entering the element from one node at any time t is equal to the current leaving the element from the other node at t.

For $\mathcal{S}_3$, KCL states:

$$i_1(t) + i_4(t) + i_5(t) + i_6(t) = 0$$

For $\mathcal{S}_4$, KCL states:

$$i_3(t) + i_{11}(t) + i_8(t) + i_9(t) - i_6(t) - i_5(t) - i_4(t) = 0$$

For $\mathcal{S}_5$, KCL states:

$$i_{11}(t) - i_{10}(t) - i_4(t) - i_7(t) = 0$$

Note that these are the four currents pertaining to the op amp. Thus choosing a gaussian surface which encloses any n-terminal element, we state that the algebraic sum of the currents leaving or entering the n-terminal element is equal to zero at all times t. This fact will be used in the next section when we discuss n-terminal elements.

For $\mathcal{S}_6$, we have

$$-i_{12}(t) - i_3(t) - i_{11}(t) - i_8(t) - i_9(t) = 0$$

Note that $\mathcal{S}_6$ contains only the datum node ⑤.

We state KCL for nodes:

> *KCL (node law)* For all lumped circuits, for all times t, the algebraic sum of the currents *leaving* any node is equal to zero.

REMARK Although a node is a special case of a gaussian surface, KCL for nodes is far more useful than the general statement in terms of gaussian surfaces. Equations written for nodes from the node law are subsets of the equations written for gaussian surfaces of a given circuit. Yet as we shall see in Sec. 6, KCL equations for nodes lead easily to simple analytic formulation of KCL and are the key idea in the node analysis of Chap. 5.

4.4 Three Important Remarks

1. KVL and KCL are the two fundamental postulates of lumped-circuit theory.
2. KVL and KCL hold irrespective of the *nature* of the elements constituting the circuit. Hence, we may say that Kirchhoff's laws reflect the *interconnection* properties of the circuit.
3. KVL and KCL always lead to *homogeneous linear algebraic* equations with *constant real coefficients*, 0, 1, and -1, if written in the fashion given in this section.

5 FROM CIRCUITS TO GRAPHS

The interconnection properties of a circuit can best be exhibited by way of a graph, called a *circuit graph*. In this section, we will demonstrate how a graph can be obtained from a circuit. The graph retains all the interconnection properties of the circuit but suppresses the information on the circuit elements. Therefore, as far as KVL and KCL are concerned, the circuit graph is all that we need.

A *graph* $\mathcal{G}$ is specified by a set of nodes $\{①, ②, \ldots, ⓝ\}$ together with a set of branches $\{\beta_1, \beta_2, \ldots, \beta_b\}$. If each branch is given an orientation, indicated by an arrow on the branch, we call the graph directed, or, simply, a *digraph*. In Fig. 5.1, we show a connected digraph with five nodes and seven

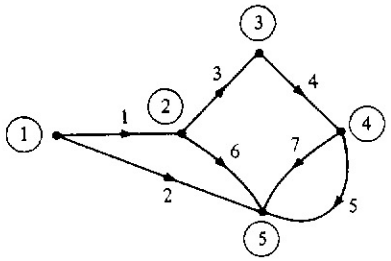

Figure 5.1 A digraph with five nodes and seven branches.

branches, i.e., $n = 5$ and $b = 7$. The *arrows* on the branches are used to denote the reference directions of the currents.

5.1 The Element Graph: Branch Currents, Branch Voltages, and the Associated Reference Directions

A two-terminal element, shown in Fig. 5.2*a*, can be represented by a graph with two nodes and one branch. This graph is called the *element graph* of the two-terminal element. By KCL, the current i flowing from node ① into the element is equal to the current leaving the element by node ②. We therefore represent a two-terminal element by a digraph with the arrow on the branch indicating the reference direction of the current a shown in Fig. 5.2*b*. By doing so we have suppressed the circuit element; and, as such, the current i is called the *branch current* of the two-terminal element.

The voltage across the element is the voltage v between the node-pair ①, ② shown in Fig. 5.2*a*. The voltage v is called the *branch voltage* of the two-terminal element. The reference direction is specified by the + and − signs associated with node-pair ①, ②. Thus the branch voltage $v(t) > 0$ if and only if, at time t, the potential of node ① is larger than that of node ②. Similarly, the branch current $i(t) > 0$ if and only if, at time t, the current enters the element by node ① and leaves it by node ②. When, for the two-terminal elements shown, the current and voltage reference directions are chosen as in Fig. 5.2*a*, we say that we have chosen associated reference directions for that two-terminal element.

More precisely, the *associated reference directions* are defined as follows: Suppose that the voltage reference direction is chosen; then the current

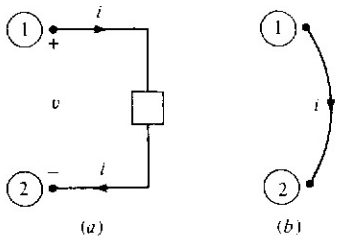

Figure 5.2 (*a*) A two-terminal element and (*b*) its digraph representation.

reference direction is always selected so that the arrow is directed from the + sign toward the − sign through the element. Or, if the reference direction for the current is chosen, the voltage reference direction is specified with the + sign at the node where the current enters the element. This is the convention we will follow throughout, giving us the distinct advantage of not having to mark the signs for the voltage reference direction any more. Therefore in Fig. 5.2*b*, we show only the arrow on the digraph.

Associated reference directions have a very useful property, namely, they make the accounting of power flow quite easy. For the two-terminal element of Fig. 5.2:

$$p(t) \triangleq v(t)i(t) \qquad (5.1)$$
$$= \textit{power} \text{ delivered at time } t \textit{ to} \text{ the two-terminal element } \textit{by} \text{ the remainder of the circuit to which it is connected}$$

If the voltage $v(t)$ is expressed in *volts* and the current in *amperes*, then the power is expressed in *watts*.

Three-terminal elements The digraph representation of two-terminal elements discussed above can be extended to three-terminal elements. For a three-terminal element as shown in Fig. 5.3, there are three node currents i_1, i_2, and i_3, and three voltages v_{1-3}, v_{3-2}, and v_{2-1}. However, from KVL we know that $v_{1-3} + v_{3-2} + v_{2-1} = 0$; and therefore only two voltages can be specified independently. So let us choose arbitrarily node ③ as the datum node and use the node-to-datum voltages for nodes ① and ② as the two independent voltages. Similarly, from KCL, we know that $i_1 + i_2 + i_3 = 0$. Therefore, for the datum node chosen at ③, we use i_1 and i_2 as the two independent currents.

The digraph representation of a three-terminal element with node ③ as datum is shown in Fig. 5.4. Note that it contains *two* branches and three nodes. The arrows indicate the current reference directions for i_1 and i_2. The two currents i_1 and i_2 are called the *branch currents* of the three-terminal element. Using the associated reference directions for the voltages, we redraw the three-terminal element as shown in Fig. 5.5 and define $v_1 = v_{1-3}$ and $v_2 = v_{2-3}$

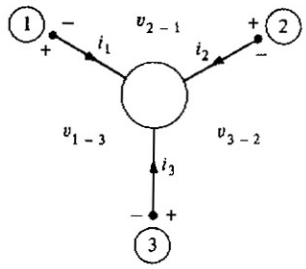

Figure 5.3 A three-terminal element.

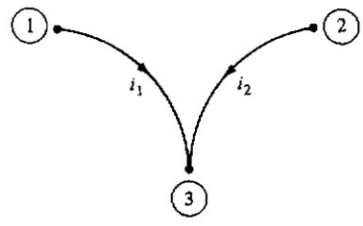

Figure 5.4 The digraph representation of a three-terminal element with node ③ chosen as datum.

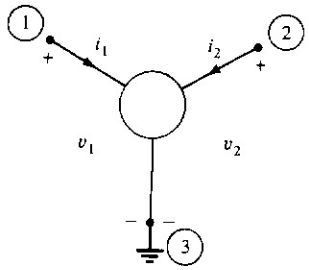

Figure 5.5 A three-terminal element with branch currents i_1, i_2 and branch voltages, v_1, v_2 using associated reference directions.

as the two *branch voltages* of the three-terminal element. Thus by using the digraph representation, we have extended the *circuit variables*: branch voltages and branch currents from two-terminal elements to three-terminal elements.

Obviously, for a three-terminal element, there exist altogether three possible digraph representations depending on which node is chosen as the datum node. In addition to the digraph in Fig. 5.4 we have two other digraphs as shown in Fig. 5.6.

***n*-Terminal elements** We can easily generalize the above to n-terminal elements as shown in Fig. 5.7. Thus for an n-terminal element, we have an

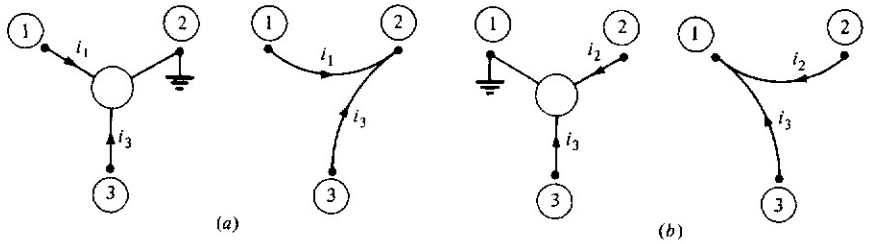

Figure 5.6 Other digraph representations of a three-terminal element: (*a*) Datum node, ②; (*b*) datum node, ①.

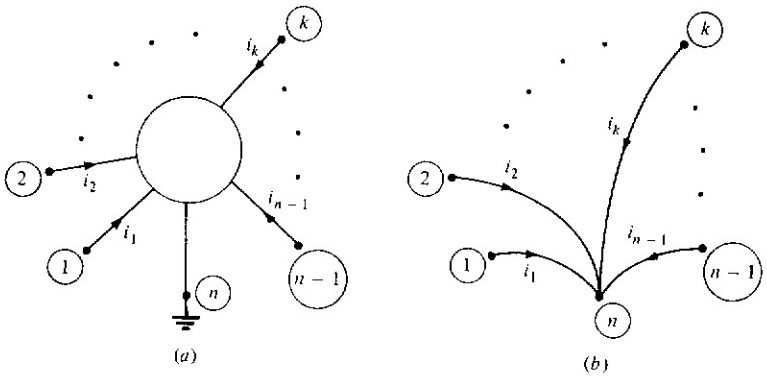

Figure 5.7 An n-terminal element and its element graph with node ⓝ as datum node.

element graph with $n-1$ branches and n nodes. There are $n-1$ branch currents and $n-1$ branch voltages; and we always use the associated reference directions and choose the current reference directions as shown, i.e., with arrows entering the element at the nodes. The *power* delivered to the element from the outside to the element at time t is therefore

$$p(t) = \sum_{k=1}^{n-1} v_k(t) i_k(t) \tag{5.2}$$

5.2 The Circuit Graph: Digraph

For a given circuit, if we replace each element by its element graph, the result is a directed *circuit graph*, or simply a *digraph*.

For example, a digraph associated with the circuit in Fig. 4.3 is the one shown in Fig. 5.1. We may now use the digraph instead of the circuit to write equations of KVL and KCL. It is interesting to note that since the circuit contains a three-terminal element, the digraph bears little resemblance to the circuit. In fact, given the digraph, without specifying which nodes belong to the three-terminal element, it is not possible to reconstruct the circuit. This observation is not true if the circuit contains only two-terminal elements.

Exercise 1 Demonstrate that the op-amp circuit in Fig. 4.4 has its associated digraph shown in Fig. 5.8 if node ⑤ is chosen as the datum node for the op amp.

Note that in the circuit there are seven two-terminal elements and one four-terminal element. The total number of branches in the digraph is equal to $7+(4-1)=10$. (Remember for an n-terminal element, the element graph has $n-1$ branches.)

Exercise 2 Choosing note ⑤ as the datum node for the circuit, show by KVL that one can express all 10 branch voltages $v_1, v_2, \ldots, v_{10}$ in terms of

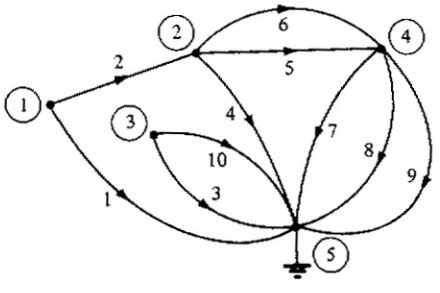

Figure 5.8 Digraph associated with the circuit in Fig. 4.4. The branches are numbered according to the corresponding currents in Fig. 4.4.

the four node-to-datum voltages e_1, e_2, e_3, and e_4 as follows:

$$\begin{aligned} v_1 &= e_1 \\ v_2 &= e_1 - e_2 \\ v_3 &= e_3 \\ v_4 &= e_2 \\ v_5 &= e_2 - e_4 \\ v_6 &= e_2 - e_4 \\ v_7 &= e_4 \\ v_8 &= e_4 \\ v_9 &= e_4 \\ v_{10} &= e_3 \end{aligned} \tag{5.3}$$

Exercise 3 Show that KCL equations written for the four nodes ① to ④ are

$$\begin{aligned} i_1 + i_2 &= 0 \\ -i_2 + i_4 + i_5 + i_6 &= 0 \\ i_3 + i_{10} &= 0 \\ -i_5 - i_6 + i_7 + i_8 + i_9 &= 0 \end{aligned} \tag{5.4}$$

Exercise 4 Express Eqs. (5.3) and (5.4) in matrix form using the vectors $\mathbf{v}$, $\mathbf{e}$, and $\mathbf{i}$, e.g., $\mathbf{v} = [\mathbf{v}_1, \mathbf{v}_2, \ldots, \mathbf{v}_{10}]^T$, where the superscript T denotes matrix transposition.

REMARK The fundamental concept of using a circuit graph instead of the circuit itself in writing KVL and KCL equations is the following:

1. We convert circuit elements whether two-terminal, three-terminal, or n-terminal into *branches*, thus we were able to define *branch voltages* and *branch currents* for any element in a circuit.
2. With a circuit graph we can define precisely the interconnection properties of a circuit using the branch-node incidence relation of a graph to be discussed in Sec. 6.

Exercise 5 Show that if branch 3 in Fig. 4.4 is replaced by a short circuit thereby coalescing nodes ③ and ⑤ into one node, then the digraph in Fig. 5.8 will contain a *self-loop*, i.e., a loop made of one branch and one node.

5.3 Two-Ports, Multiports, and Hinged Graphs

Up to now we have assumed that the circuit is connected. In Fig. 3.2*b* the circuit, because of the presence of a two-winding transformer, is not connected. It turns out that we can easily take care of the situation; but before we do so, we need to introduce a special class of four-terminal elements called two-ports. A *two-port* is a circuit element or a circuit with two *pairs* of *accessible* terminals. Thus a two-port may contain many circuit elements.

Two-ports In many engineering situations the terminals of a multiterminal device are naturally associated in pairs: For example, in a hi-fi chain the input pair is connected, say, to a microphone and the output pair to a loudspeaker system. These pairs of associated terminals are called *ports*. Another example is a two-winding transformer: The two input terminals constitute a natural *input port* and the two output terminals constitute a natural *output port*. In either case, the typical connections to the four-terminal element have the form shown in Fig. 5.9. Note the labeling of the nodes and the currents: the input pair is ①, ①′ and the output pair is ②, ②′.

When we view the four-terminal element of Fig. 5.9 as a *two-port*, we consider *only* the voltages v_1 and v_2 and the four terminal currents i_1, i_1', i_2, i_2'. Naturally, v_k is called the *port voltage* at port ⓚ, $k = 1, 2$. Now the gaussian surfaces $\mathcal{S}_1$ and $\mathcal{S}_2$ shown in Fig. 5.9 and KCL impose the two current constraints:

$$i_1 = i_1' \qquad \text{and} \qquad i_2 = i_2'$$

The point is that these two port constraints reduce the number of current variables from four to two: i_1 and i_2. The current i_k is called the *port current* at port ⓚ.

Note that at each port the port voltage v_k and the port current i_k have associated reference directions: Hence $v_k(t)i_k(t)$ is the power entering port k at time t. For example, the power delivered at time t, *by* the remainder of the circuit *to* the two-port of Fig. 5.9 is given by

$$v_1(t)i_1(t) + v_2(t)i_2(t)$$

Naturally, a two-terminal element may be viewed as a one-port. Thus, in generalizing the digraph representation from a one-port to a two-port, we use two branches and four nodes for its element graph as shown in Fig. 5.10.

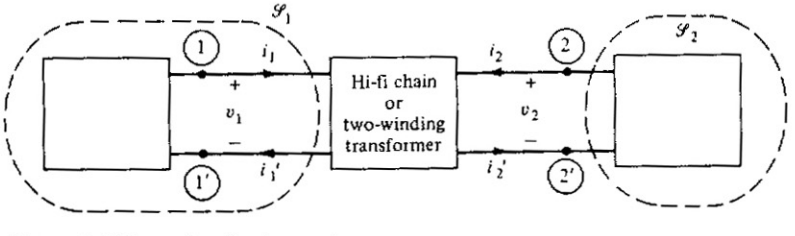

Figure 5.9 Example of a two-port.

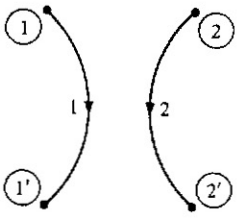

Figure 5.10 The element graph of a two-port.

Therefore the port voltages v_1 and v_2 are also referred to as the branch voltages of the two-port. Similarly, we can also call the port currents i_1 and i_2 the branch currents of the two-port. This is in contrast to a four-terminal element where there are three branches in its element graph, thus three branch voltages and three branch currents.

Multiports We can generalize the concept of two-ports to multiports. For example, a three-winding transformer is a three-port as shown in Fig. 5.11. Its element graph has three branches and six nodes as shown in Fig. 5.11*c*. The three branch voltages and three branch currents are the port voltages and port currents, respectively, for the three-port.

Hinged graphs The element graph of a two-port consists of two branches which are not connected. It signifies that the port voltages or port currents at different ports are not related because of connections but rather are *coupled* because of physical phenomena within the element. For example, the trans-

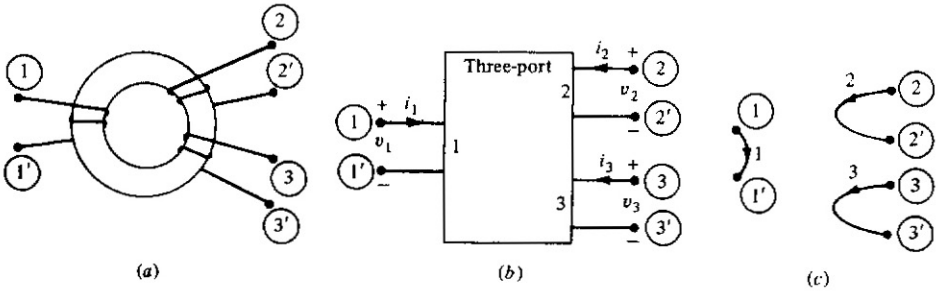

Figure 5.11 (*a*) A three-winding transformer. (*b*) the corresponding three-port, and (*c*) its element graph.

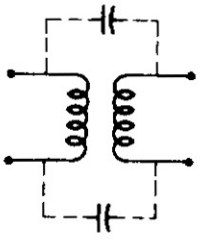

Figure 5.12 A model of a physical transformer which includes two parasitic capacitors.

former port voltages are coupled magnetically via the flux linkages among the various windings. Therefore circuits containing two-ports or multiports have circuit graphs which are often unconnected.[6]

To avoid an "unconnected" circuit graph, we can tie together the two separate ports of a circuit graph at two arbitrary nodes by a branch. This is illustrated in Fig. 5.13*a*, where nodes ③ and ⑤ are tied together by a branch k. This connection does not change any branch voltage or current in the original circuit. This is easily seen because, by using KCL with a gaussian surface which encloses one of the separate parts of the graph and which cuts branch k, the current i_k is zero. If $i_k = 0$, it amounts to an open circuit or no connection; thus we have not changed the behavior of the circuit. Next, since voltages are measured between nodes, we choose a datum node for each separate part. If we choose nodes ③ and ⑤ as the datum nodes for the separate parts, we may "solder" together node ③ and node ⑤ as shown in Fig. 5.13*b* to make them the common datum. The graph so obtained is called a *hinged graph*. With the introduction of the concept of a hinged graph, we have generalized our treatment so far to include two-ports and multiports, that is, we can always assume without loss of generality that any lumped circuit and its circuit graph are *connected*.

"Grounded" two-ports If a common connection exists between nodes ① and ② of a two-port as shown by the low-pass filter in Fig. 5.14*a*, we call it, by tradition, a "*grounded*" *two-port*. The word "grounded" does not necessarily mean that the node is always set to zero potential. Rather, a "grounded" two-port is essentially a three-terminal element with its datum node specified as the common node of the two-port. Obviously, the element graph for a "grounded" two-port consists of two branches which are tied together at the common node shown in Fig. 5.14*b*.

Similarly, an n-terminal element can be viewed as a "grounded" $(n-1)$-port if the datum is specified.

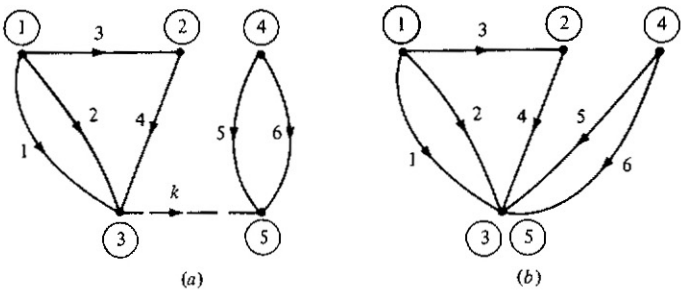

Figure 5.13 (*a*) Connecting nodes ③ and ⑤ by a branch k. (*b*) Soldering together nodes ③ and ⑤ to obtain a hinged graph.

[6] An exception to this is, for example, in modeling a physical transformer; we may need to use additional elements to tie the windings together as shown in Fig. 5.12.