1. (Circuit Review) (15 pts)

a) Find $V_{\text{out}}$.
b) Find the Thevinin equivalent circuit.

2. (Transient Review) (15 pts)

In the circuit above, switch is open for $t < 0$, then closed at $t = 0$ then opened again at $t = 10\text{ms}$.

a) Determine $v_c(t)$ for $t > 0$.
b) Sketch $v_c(t)$ for $t > 0$.

3. (Op Amp Review) (15 pts)

Determine the Thevinin Equivalent with respect to terminals A and B.

4. (Diode Review) (15 pts)

a) Plot $V_{\text{out}}$ vs $V_{\text{in}}$. Diode is ideal with $V_{\text{on}} = 0.6V$.
b) Let $V_{\text{in}}(t) = 5\cos(2\pi t)$. Plot $V_{\text{out}}(t)$. 
5. (Logic Design Review) (15 pts)
Consider a logic function $F$ which has three inputs $A, B, C$. The function $F$ is false when all inputs are false, or all inputs are true. Otherwise $F$ is true.

a) List the truth table for $F$.
b) Use a Karnaugh map to find the minimal-sum-of-products form for $F$.
c) Draw the logic diagram for $F$ minimal sum-of-products using minimal NAND, NOR, and NOT gates.
d) Draw a timing diagram, assuming unit gate delays. $ABC$ follows the sequence 100, 111, 110, 001, 000, 011, 101, changing to each next value after a unit delay.
e) Draw the circuit diagram for part c) using PMOS and NMOS transistors in standard CMOS gates.

6. (Op Amp review) (20 pts)

\[
\begin{align*}
R_6 &= 100K\Omega, \\
C_4 &= 100nF, \\
R_7 &= 10K, \\
R_8 &= 20K, \\
V_1 &= \pm10V.
\end{align*}
\]

a) Plot $V_o$ vs $v_T$. (Note op amp labelled “comp” is not running in negative feedback).
b) Sketch $v_T(t)$.

7. (Load Line Review) (15 pts)

version A

\[
\begin{align*}
I_o &= 1.0mA, \\
R &= 5K\Omega.
\end{align*}
\]

a) Estimate possible operating points for $I, V$.
b) By hooking up some external components and switch(es), could you change from one operating point to another? (By the way, this is an obscure kind of flip-flop.)

8. (Phasor Review/Class D Output) (15 pts)

\[
\begin{align*}
L_1 &= 20\mu H, \\
C_1 &= 0.5\mu F, \\
R_1 &= 4\Omega, \\
V_{in} &= 50\cos\omega t.
\end{align*}
\]

a) Write expressions for $|V_L(\omega)|$ and phase $V_L(\omega)$.
b) Sketch $|V_L(\omega)|$ and phase $V_L(\omega)$.
c) Determine a good value for $\omega$ so that the filter would block just about all of the cosine term, e.g. $|V_L| < 0.001$ V.