Back-of-Envelope

Inspection Method

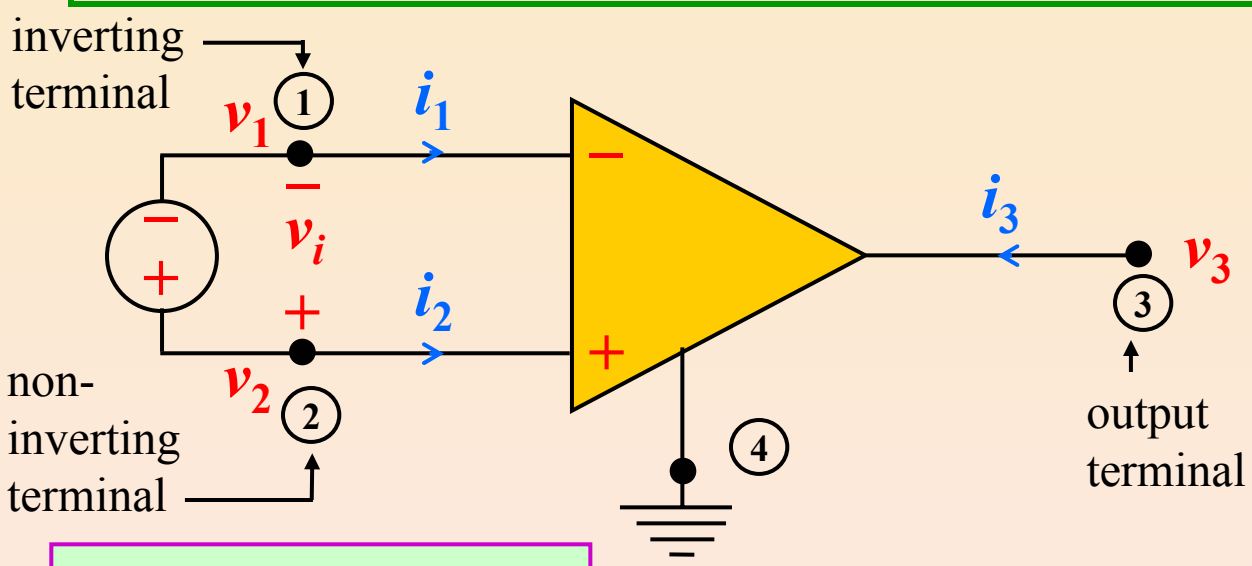
Assume

then

Validate

Method

Ideal Operational Amplifier (Op Amp)



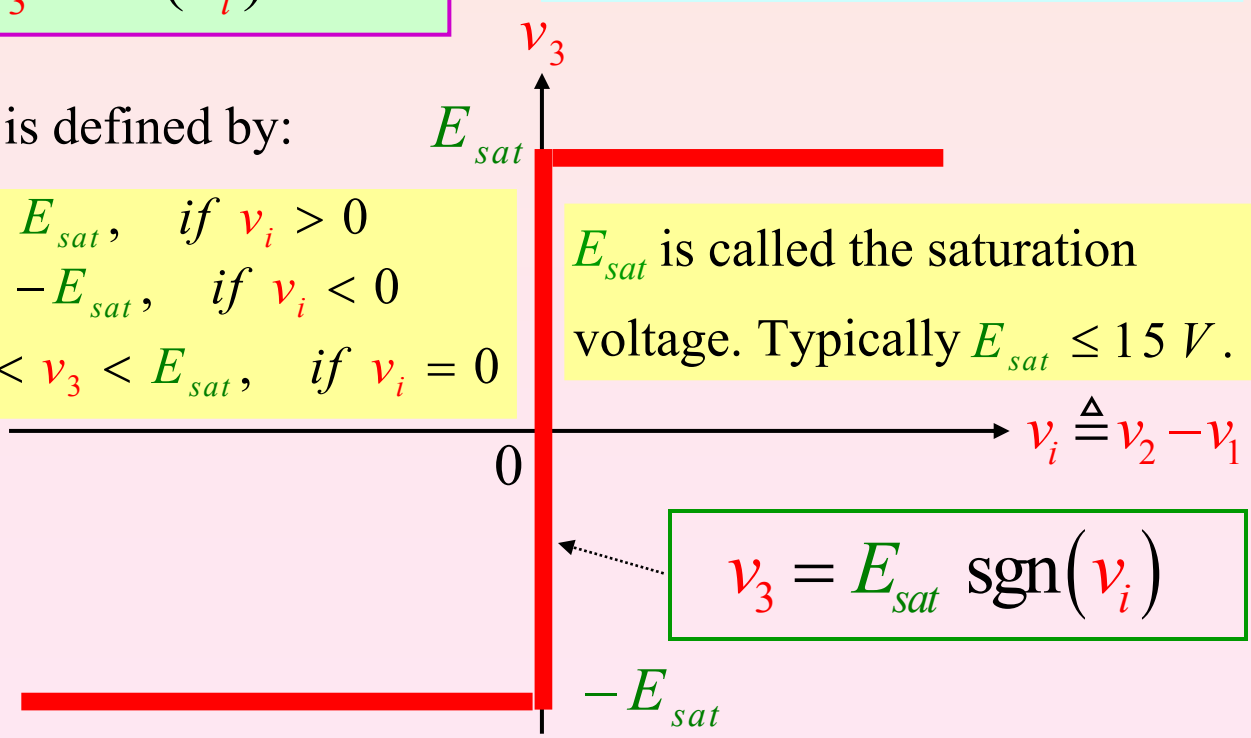
$$i_1 = 0$$
$$i_2 = 0$$
$$v_3 = \mathbf{F}(v_i)$$

The nonlinear relationship **F** depends only on $v_i \triangleq v_2 - v_1$

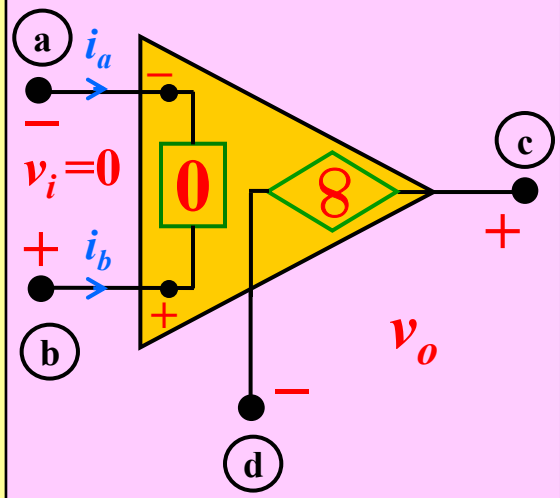
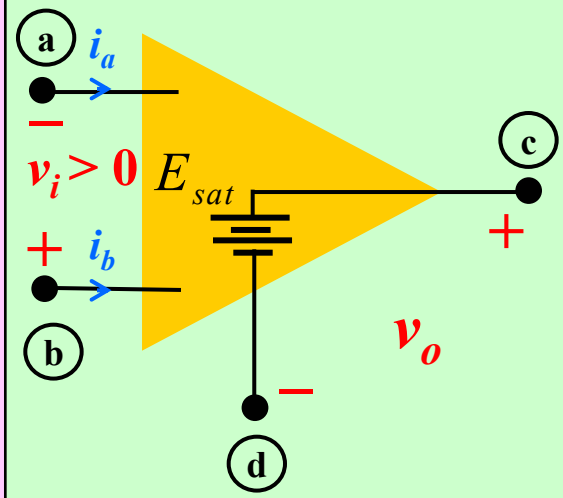
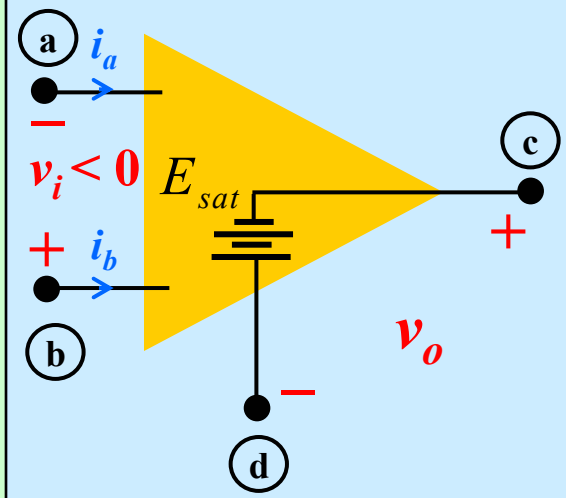
F (v_i) is defined by:

$$v_3 = E_{sat}, \quad if \ v_i > 0$$
$$v_3 = -E_{sat}, \quad if \ v_i < 0$$
$$-E_{sat} < v_3 < E_{sat}, \quad if \ v_i = 0$$

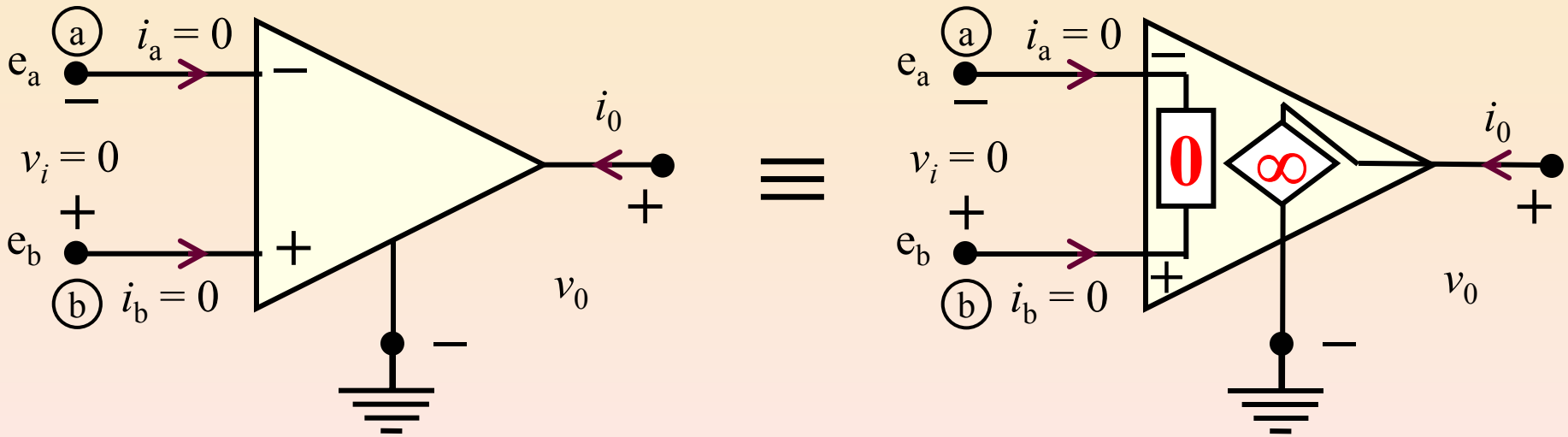
E_{sat} is called the saturation voltage. Typically $E_{sat} \le 15\ V$.



$$v_3 = E_{sat}\ \mathrm{sgn}(v_i)$$

Operating Region	**Linear Region**	**+ Saturation Region**	**- Saturation Region**
op amp Circuit Model			
op amp Equation	$i_a = 0$ $i_b = 0$ $v_i = 0$	$i_a = 0$ $i_b = 0$ $v_o = E_{sat}$	$i_a = 0$ $i_b = 0$ $v_o = -E_{sat}$
Validating Inequality	$-E_{sat} < v_o < E_{sat}$	$v_i > 0$	$v_i < 0$

OP AMP in Linear Region



OP AMP Element Laws
(Linear Region)

$$i_a = 0$$
$$i_b = 0$$
$$v_i \triangleq e_b - e_a = 0$$

Remark

i_0 and v_0 can assume any value determined by the external circuit

Simple Op Amp Circuit Analysis :

3 Common Steps

Step 1. *Assume Op Amp Regime*

Replace *Op Amp* by circuit model for the assumed regime.

Step 2. Solve the resulting *linear resistive* circuit

3 typical problems:

- find operating point
- derive and sketch DP plot
- derive and sketch TC plot

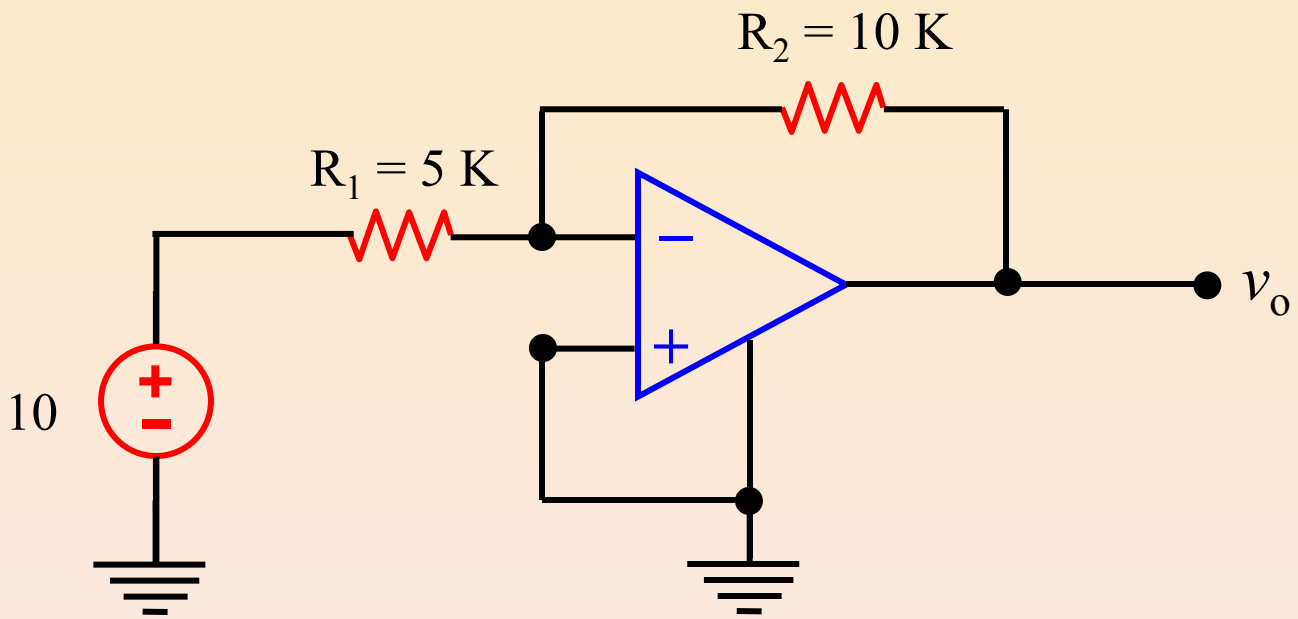
Step 3. Derive the *dynamic range* of the Op Amp's assumed operating regime

Derive the *op-amp regime validation variable* (v_i ,for *linear* regime, and v_o, for $\pm$ *saturation* regimes) and apply the *regime validation inequality*.

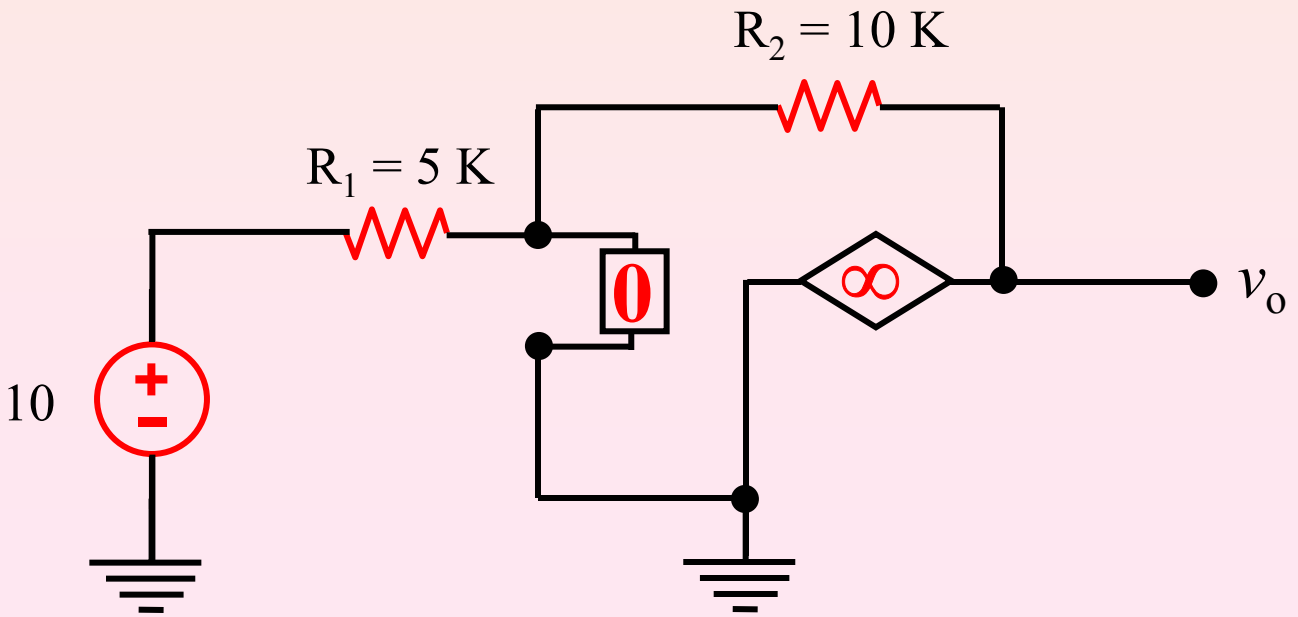
5 Analysis Steps within each Regime

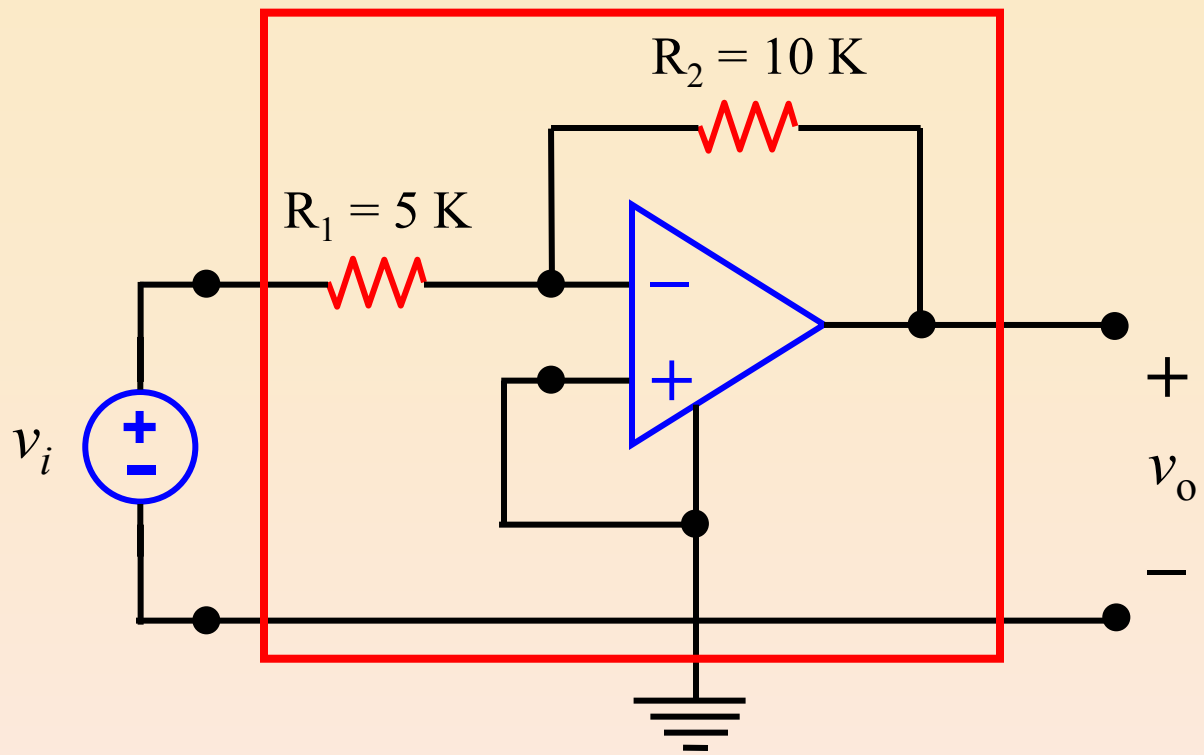
1. Express the *current* of *each resistor* in terms of its node-to-datum voltages, via *Ohms law* and *KVL*.
2. Apply KCL to *all* nodes except the *ground* (datum) node, and the *op amp output* node.
3. Solve for the desired variable.
4. Solve for the op amp *regime validation variable* (v_i, for *linear* regime, v_i, for $\pm$ *saturation* regimes) as a function of the driving-point voltage (or current).
5. Apply the appropriate *regime validation inequality* and calculate the *dynamic range* in terms of the *driving-point voltage* v (i.e., $v_a \leq v \leq v_b$), or in terms of the *driving-point current* i (i.e., $i_a \leq i \leq i_b$).

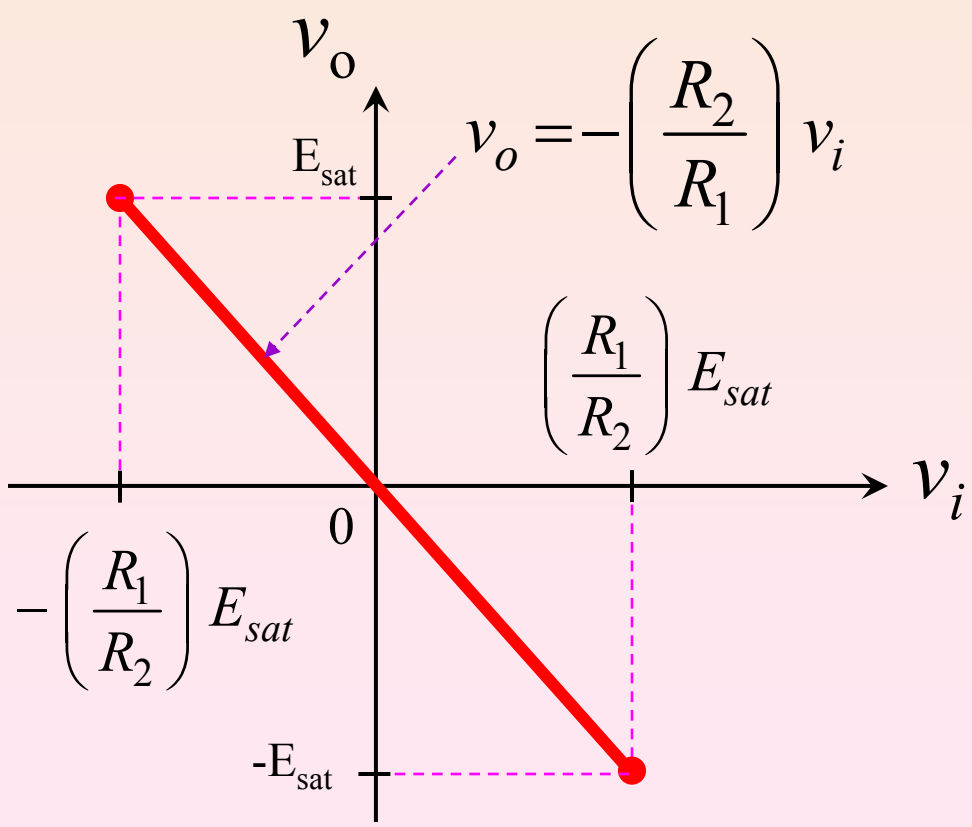
Find Output Voltage v_o for Op amp operating in the Linear Region



Replace Op amp by Model in *Linear Regime*




R2 = 10 K
R1 = 5 K
vi
+
vo
−


vo
Esat
vo = −(R2/R1) vi
(R1/R2) Esat
vi
0
−(R1/R2) Esat
-Esat

Validation

Find a *dynamic range* of the *driving-point voltage* v_i where op amp is operating in the assumed linear regime.

Validation Inequality:

$$-E_{sat} < v_0 < E_{sat}$$

since

$$v_o = -\left(\frac{R_2}{R_1}\right) v_i$$

$$-E_{sat} < -\left(\frac{R_2}{R_1}\right) v_i < E_{sat}$$

Right inequality : $v_i > -\left(\frac{R_1}{R_2}\right) E_{sat}$

Left inequality : $v_i < \left(\frac{R_1}{R_2}\right) E_{sat}$

Op amp circuit realization of linear controlled sources

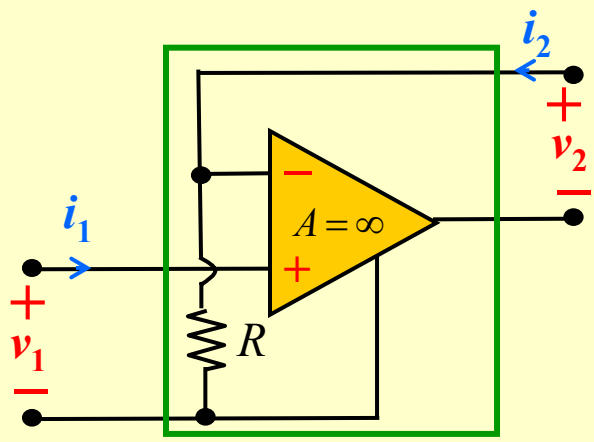
$$i_1 = 0$$
$$i_2 = g\, v_1$$

$$g \triangleq \frac{1}{R}$$

dynamic range:

$$v_2 - E_{sat} < v_1 < v_2 + E_{sat}$$

VCCS



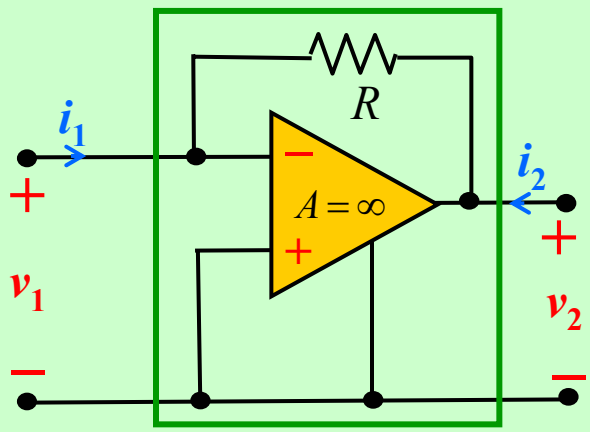
$$v_1 = 0$$
$$v_2 = r\, i_1$$

$$r \triangleq -R$$

dynamic range:

$$-\frac{E_{sat}}{R} < i_1 < \frac{E_{sat}}{R}$$

CCVS



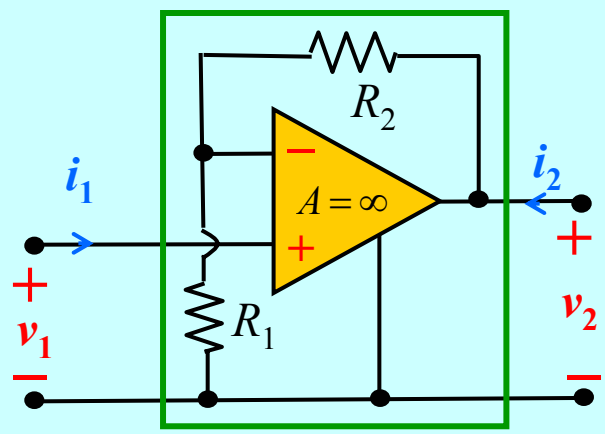
$$i_1 = 0$$
$$v_2 = \mu\, v_1$$

$$\mu \triangleq 1 + \frac{R_2}{R_1}$$

dynamic range:

$$-\left(\frac{R_1}{R_1 + R_2}\right) E_{sat} < v_1 < \left(\frac{R_1}{R_1 + R_2}\right) E_{sat}$$

VCVS



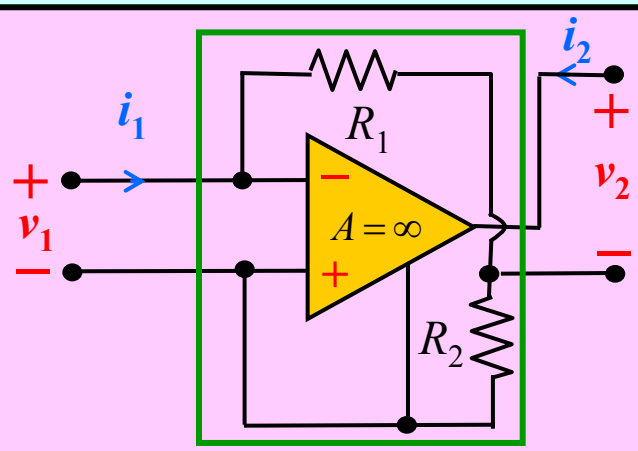
$$v_1 = 0$$
$$i_2 = \alpha\, i_1$$

$$\alpha \triangleq 1 + \frac{R_1}{R_2}$$

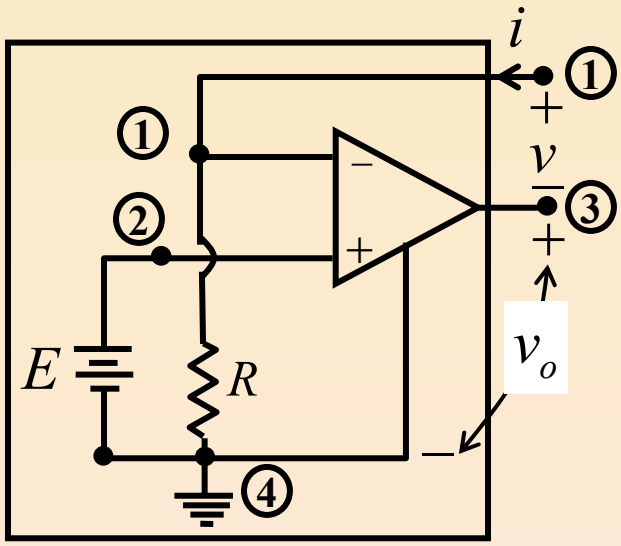
dynamic range:

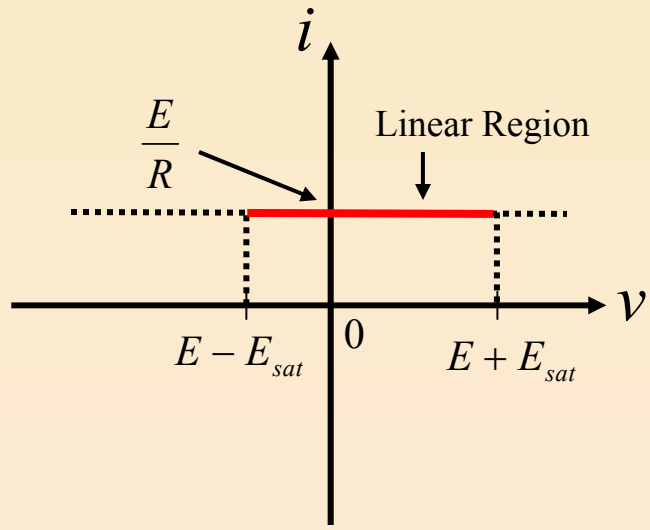
$$\left(\frac{v_2 - E_{sat}}{R_1}\right) < i_1 < \left(\frac{v_2 + E_{sat}}{R_1}\right)$$

CCCS

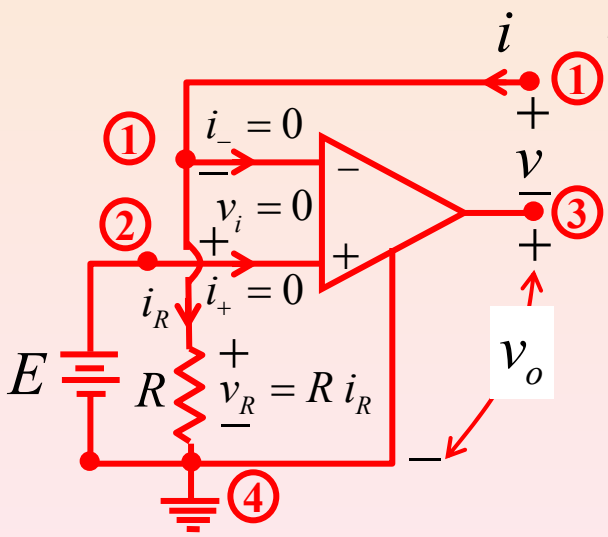


DP Plot of an *op-amp* VCCS Circuit





Linear Region



Step 1: Derive an equation relating v and i across terminals ①–③ (DP plot in the linear region) :

$$i = i_R \tag{1}$$

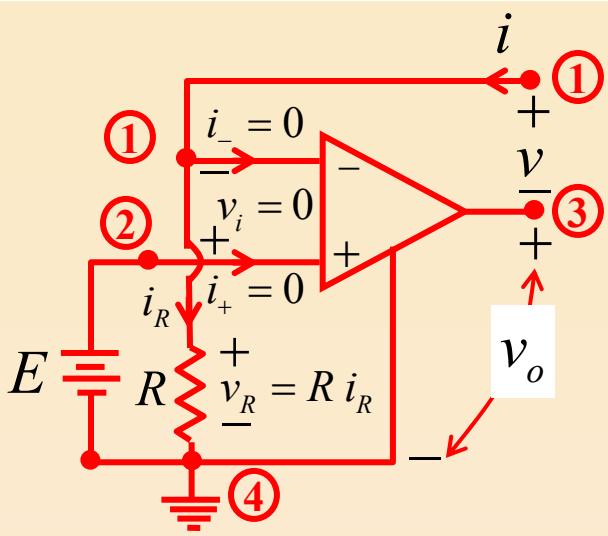
$$v_R = E = R\, i_R \tag{2}$$

Substitute (2) into (1) :

$$i = \frac{E}{R} = 0 \bullet v + \frac{E}{R} \tag{3}$$

This equation describes the Norton equivalent circuit across terminals ①–③ $\left(i = G_{eq} v + i_{sc}\right)$,

$$\therefore \boxed{G_{eq} = 0\,, \quad i_{sc} = \frac{E}{R}} \tag{4}$$



Step 2: *Validation* : $\boxed{-E_{sat} < v_o < E_{sat}}$

To test the above condition for the op amp to be operating in the linear region, we must derive an equation relating v_o and v :

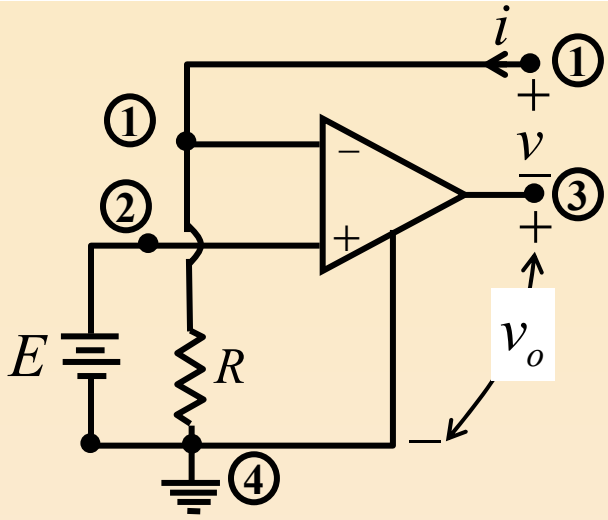
Apply KVL around closed node sequence ①−③−④−②−① :

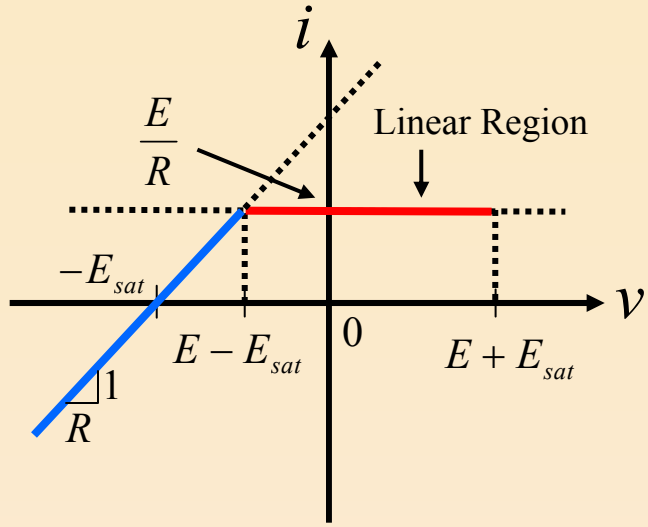
$$v + v_o - E - v_i = 0 \tag{5}$$

$$\Rightarrow \; v_o = E - v \tag{6}$$

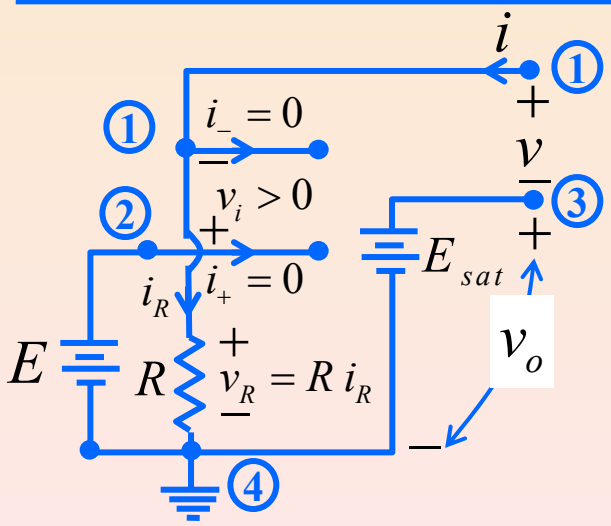
Hence, $-E_{sat} < v_o < E_{sat}$ implies

$$\boxed{-E - E_{sat} < v < E + E_{sat}} \tag{7}$$





+ Saturation Region



Step 1: Derive an equation relating v and i (DP plot in the + saturation region) :

Apply KVL around closed-node sequence ①−②−④−③−① :

$$\boxed{v = Ri - E_{sat}} \qquad (8)$$

Step 2: *Validation* : $\boxed{v_i > 0}$

To test the above condition for the op amp to be operating in the + saturation region, we must derive an equation relating v_i and v :

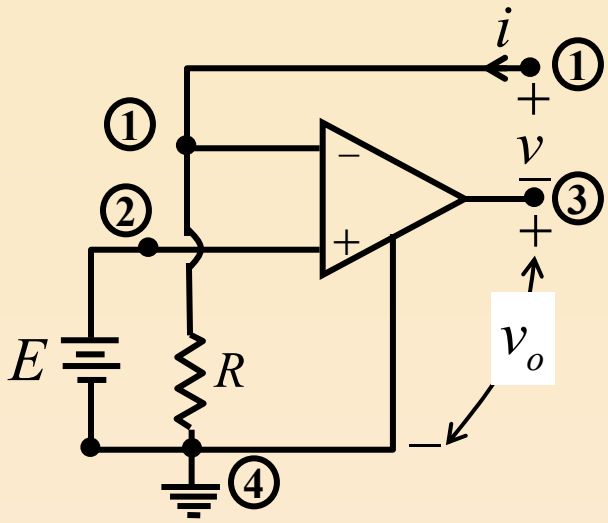
Apply KVL around closed node sequence ①−②−④−③−① :

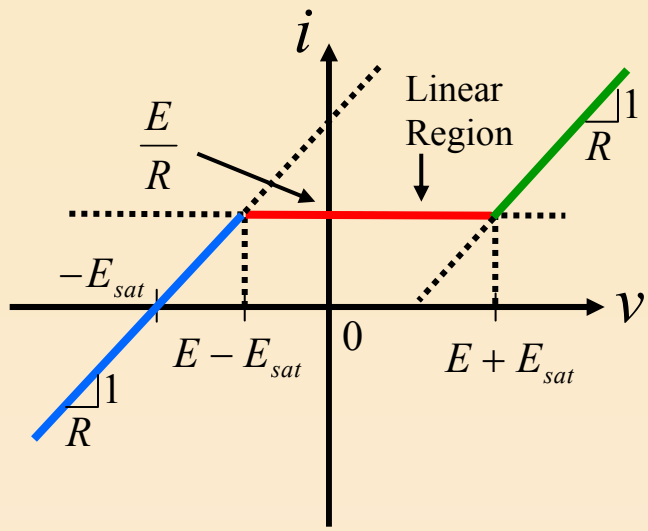
$$-v - v_i + E - E_{sat} = 0$$

$$\Rightarrow \; v_i = -v + E - E_{sat} \qquad (9)$$

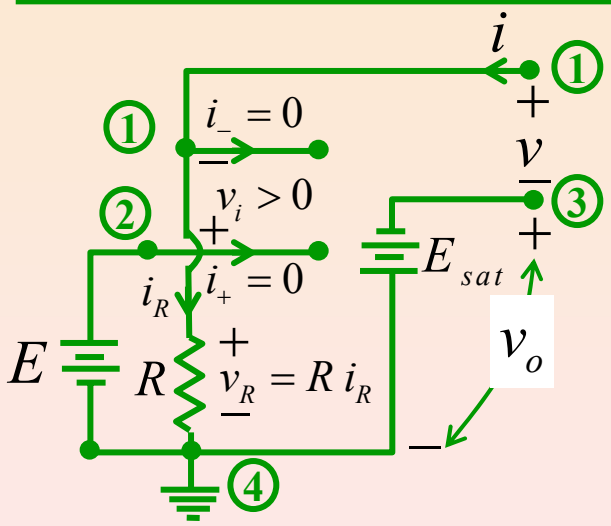
Hence, $v_i > 0$ implies

$$\boxed{v < E - E_{sat}} \qquad (10)$$





- Saturation Region



Step 1: Derive an equation relating v and i (DP plot in the - saturation region) :

Apply KVL around closed-node sequence ①−②−④−③−① :

$$\boxed{v = Ri + E_{sat}} \qquad (11)$$

Step 2: *Validation* : $\boxed{v_i < 0}$

To test the above condition for the op amp to be operating in the - saturation region, we must derive an equation relating v_i and v :

Apply KVL around closed node sequence ①−②−④−③−① :

$$-v - v_i + E + E_{sat} = 0$$

$$\Rightarrow \; v_i = -v + E + E_{sat} \qquad (12)$$

Hence, $v_i < 0$ implies

$$\boxed{v > E + E_{sat}} \qquad (13)$$

Remark

The above **op-amp** circuit functions as a **VCCS** defined by

$$\boxed{\begin{aligned} i_1 &= 0 \\ i_2 &= G_{21}\, v_1 \end{aligned}} \tag{14}$$

Upon defining

$$\boxed{\begin{aligned} v_1 &\triangleq E \\ i_1 &= 0 \\ i_2 &= i \\ G_{21} &\triangleq \frac{E}{R} \end{aligned}} \tag{15}$$

It is valid over the voltage range

$$\boxed{-E - E_{sat} < v_2 < E + E_{sat}} \tag{16}$$