1. a) 

\[
\begin{align*}
00 & \quad \text{or} \quad 10 \\
11 & \quad 01
\end{align*}
\]

b) If \(Q_1Q_0\) starts with \((1,1)\) or \((0,0)\), it will finally go to \((0,0)\) so the frequency is 0 Hz.

If \(Q_1Q_0\) starts with \((0,1)\) or \((1,0)\), the frequency will be half of clock frequency = 500 kHz.

c) Duty factor = 0% for the first case, and = 50% for the second case.

2. a) 

\[
\begin{align*}
001 & \quad \text{or} \quad 111 \\
110 & \quad 011 \\
101 &
\end{align*}
\]

b) \(f_{Q2} = 1 \text{ MHz}/2 = 500 \text{ kHz.}\)

c) 50% because in 50% of the cycle, \(Q_2\) is high (see state diagram).
3. a) 

b) For the first case, frequency = 1 MHz/2 = 500 kHz.
For the second case, frequency = 1 MHz/6 = 166.67 kHz.
c) 50% for both cases because in 50% of the cycle, $Q_0$ is high.

4. a) $i_B \neq 0$ because $V_{BE} > 0.7$ V, so it is not cut off. $V_{CE} = 10.7$ V > 0.7 V so it is not saturated. $V_C > V_E$ so it is not reversed. It must be active.

b) $i_B + i_C = i_E$. Since $i_C = \beta i_B$, $i_B = \frac{i_E}{\beta + 1} = \frac{-0.7 + 5.7}{100 + 1} = 0.05$ mA.

c) $i_E = \frac{-0.7 + 5.7}{100} = 5$ mA

5. $Q_3$ is a PMOS, $Q_2$ is a NMOS, and $Q_1$ is a NPN BJT.
If $X = 0$, the transistor is cut off (no base current). Since $i_B = i_C = 0$, $i_E = 0$. Therefore, $Y = +10$ V and NMOS is on, $V_{out} = 0$ V (ground).

If $X = +5$ V, $i_B \neq 0$ so not cutoff. $V_C > V_B$ so it is not reversed. Now checking if it’s active: $i_B \approx \frac{5 - 1}{400} = 1$ mA. If $i_C = 100i_B = 100$ mA, $V$ across the 1 k$\Omega$ resistor = 0.1 A * 1000 $\Omega$ = 100 V, which is impossible. Therefore, the transistor is saturated and $Y = 0.3$ V (logic = “0”).
Summary:

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>$Q_3$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V</td>
<td>Cut-off</td>
<td>On</td>
<td>Off</td>
<td>0 V</td>
</tr>
<tr>
<td>5 V</td>
<td>Saturated</td>
<td>Off</td>
<td>On</td>
<td>10 V</td>
</tr>
</tbody>
</table>