Lecture 19 - MOSFETS?

Administration: Stuff on finals. Check under exams.

MOSFETS - up to 12-3 (Bias circuits inclusive of 12-3).

Recall:

\[
\text{N MOSFET} \quad \begin{cases} \text{Book:} \\
I_n \end{cases}
\]

References: (1) Microelectronics: An Integrated Approach, by Howe & Sedlin.
Nonlinear equation for an N MOS

\[ \frac{P}{V_{DS}} + I_{DS} \]

Three regions of operation:

1. Cutoff
2. Triode
3. Saturation

Goal: \( I_{DS} = f(V_{DS}, V_{GS}, \text{constant}) \)

Sketch \( I_{DS} \) vs. \( V_{DS} \)

Look at each individually
Region 1: Cutoff (NMOS is off): $V_{GS} = 0 \text{ V}$
$I_{DS} = 0 \text{ A}$

Region 2: Triode (NMOS is turning on).
$V_{GS} \geq V_{T}$ (threshold voltage, usually around 1 V)
Transistor unfortunately cannot stay in the triode region forever. Fix $V_{GS} \geq V_{TH}$. As you increase $V_{GS}$, $V_{DS} \to 0$. The effect of
This is called "pinch-off": 

Bottomline: Transistor \( I_{DS} \) reaches a maximum value 

\[ \text{Region 3: Saturation} \]

Equation: [Ref (1)]

1. \( V_{GS} \leq V_{TO}, \quad I_{DS} = 0 \ A \)

2. \( V_{GS} \geq V_{TO}, \quad I_{DS} = \frac{1}{2} \left( KP \right) \left( \frac{W}{L} \right) \left( 2 \left( V_{GS} - V_{TO} \right) V_{DS} - V_{DS}^2 \right) \)

\[ KP \quad V_{DS} \leq V_{GS} - V_{TO} \quad \text{Triede} \]
Transistor design: playing with \( \left( \frac{W}{L} \right) \)

(3) \( V_{GS} \geq V_{TO} \)

\[ I_{DS} = \left( \frac{1}{2} \right) \frac{k_p}{\mu_c} (V_{GS} - V_{TO})^2 \]

**KEY:** \( V_{DS} \geq V_{GS} - V_{TO} \) : saturation

Notice in saturation, \( I_{DS} \) is independent of \( V_{DS} \).
A transistor is actually symmetrical, if you can control the body terminal or bulk terminal.

Example:
(Q.1) Find $I_{DS}$?

Step (1): Identify gate, drain & source

Shorthand

\[ \text{GET USED TO IT} \]
Step (2): Find $V_{gs}$.

For $u_1$, $V_{gs} = V_s - V_{ds} = 2 - V_s$

Step (3): Uh... just do the problem.

Basically, you have two choices:

1. Make an EDUCATED GUESS about transistor mode of operation (triode, saturation, cut-off).
   [Hint: If you have no clue, start with saturation] (Highly unlikely)

2. Verify your guess. Correct: done!
   Incorrect: try another mode.
\[ I_{DS} = \left( \frac{K_P}{2} \right) \left( \frac{W}{L} \right) \left[ V_{GS} - V_{TH} \right]^2 \]

\[ V_S \quad \frac{V_s}{5 \, \text{V}} = \left( \frac{K_P}{2} \right) \left( \frac{W}{L} \right) \left[ 2 - V_S - 0.8 \right]^2 \]

\[ V_S \quad \frac{V_S}{5 \, \text{V}} = \left( \frac{50 \, \text{mV}}{V_S} \right) \left( 2 \right) \left( 2 - V_S - 0.8 \right)^2 \]

\[ \boxed{V_S = 6.2 \, \text{V}, \quad V_S = 0.23 \, \text{V}} \]

Note: \( V_S = 6.2 \, \text{V} \) is not good \( \Rightarrow V_{GS} = 2 - V_S \)

\( V_S = 6.2 \, \text{V} \leq 0 \)

\( \text{no} \) good
\[ V_S = 0.23 \text{ V} \checkmark \]

Check:
1. \( V_{GS} \geq V_T \), \( V_{GS} = 2 - V_S = 2 - 0.23 = 1.77 \text{ V} \)
   \( > 0.8 \text{ V} \)

2. Is the transistor saturated? \( V_{DS} \geq V_{GS} - V_T \)
   \[ V_{DS} = 1.77 - 0.8 = 0.97 \text{ V} \]

\[ I_{DS} = \frac{V_S}{5k} = \frac{0.23}{5k} = 46 \mu\text{A} \]

\[ V_D = (46 \mu\text{A})(1k) = 46 \text{ mV} \]

\[ V_D = 10 - 46 \text{ mV} = 9.954 \text{ V} \]
\[ V_{DS} = V_0 - V_S = 9.954 - 0.23 \gg 0.97 \text{ V} \]

Diagram:

- Graph with axes labeled.
- Points and lines indicating characteristics.
- Annotations noting values and conditions.

Text:

- (c) Find \( I_{DS} \).
- (A) Revise: Identify gate, drain, and source.
- Revise (c): Cross mode for forward & solve.

\[ I_{DS} = \frac{1}{2} K_P \left( \frac{V}{V} \right) (V_{GS} - V_T)^2 \]
\[ \frac{V_s}{5k} = \frac{1}{2} \left( \frac{I_0}{V_{in}} \right) (2) (2 - V_s - 0.8)^2 \]

\[ V_s = 6.23 \text{ V}, \quad V_g = 0.23 \text{ V} \]

Note: \( V_s = 6.2 \text{ V} \) is not good \( \Rightarrow \) \( V_{CS} = 2 - V_s \)

\[ = 2 - 6.2 < 0 \]

Oops, nothing happens!

\[ V_s = 0.23 \text{ V} \Rightarrow \] \( V_{CS} = 1.77 \text{ V} > 0.8 \text{ V} \)

Now, verify if transistor is saturated.
\[ V_{DS} \geq V_{GS} - V_{TO} \]
\[ 1.77V \]

\[ J_{DS} = \frac{V_S}{5 \Omega} = 46 \mu A \]

\[ V_0 = 0.5 - (1k)(46 \mu A) \]
\[ = 0.5 - 0.046V \]
\[ = 0.454V \]

\[ V_{DS} = 0.45 - 0.23 = 0.224V < 1.77V \]

Therefore, transistor is in triode region. Here, we have to go back and use triode model.
\[ I_{OS} = \frac{1}{2} (kP)^{\frac{2}{3}} \left( \frac{V_{ds}}{V} \right)^{\frac{2}{3}} \left( 2 \left( V_{ds} - V_{ds} \right) V_{ds} - V_{ds}^2 \right) \]

\[ \frac{V_s}{5k} = \frac{1}{2} \left( \frac{50uA}{w^2} \right)^{\frac{2}{3}} \left[ 2 \left( 2 - V_s - 0.8 \right) V_{ds} - V_{ds}^2 \right] \]

The problem with using the diode equation is that we need to rewrite \( V_{ds} \) in terms of \( V_s \) (our unknown).

\[ V_{ds} = V_D - V_s \quad \text{Ohm's law: } I_{OS} = \frac{0.5 - V_D}{11} \]

\[ = \left[ 0.5 - \left( \frac{11c}{V_s} \right) \right] - V_s \]

\[ = \left( 0.5 - \frac{11c V_s}{51c} \right) - V_s = 0.5 - 1.2V_s \]

\( \square \)
Therefore: \[ \frac{V_s}{5k} = \left( \frac{50 \text{ uA}}{V_s} \right) \left[ 2 \left( 2 - V_s - 0.8 \right) \left( 0.5 - 1.2 V_s \right) - (0.5 - 1.2 V_s)^2 \right] \]

\[ \Rightarrow V_s = 6.8 \text{ V} \approx 0.14 \text{ V} \]

Looks too big.

Try: \[ V_s = 0.14 \text{ V} \Rightarrow V_{gs} = 2 - 0.14 = 1.86 \text{ V} \geq V_{to} (0.8 \text{ V}) \]

Is transistor in triode region? \[ V_{DS} = 0.5 - 1.2 V_s \] (from (1))

\[ = 0.332 \text{ } V_{gs} - V_{to} \leq (1.06 \text{ V}) \]

Therefore, \[ I_{Ds} = \frac{V_s}{5k} = 28 \text{ mA} \]

\[ \text{This answer makes sense, much smaller than the } I_{Ds} \]
\[ \text{when transistor was saturated.} \]
Transistor is PSPIE:

1) Choose MbreakN3 from BREAKOUT library as shown.
(2) The next step is to define transistor parameters.

(a) Double-click on the NMOS to open the Property-Editor & enter W & L values as shown below:

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Note: Do not forget the Ms. PSpice by default uses mometers so if you enter W=2, l=1 that is a 2m x 1m NMOS, you cannot simulate a transistor that big!
(b) Close the Property Editor & right-click on the PMOS. Choose "Edit PSPICE Model" as shown below.
The PSpice model Editor pops open. Complete the model line:

```
.model Mbreakn NMOS VTO=1 KP=50e-6 lambda=0
```

This is VT "oh", not VT "zero".

Don't worry about it, just set it to zero.

(Ref: [http://www.icaen.uiowa.edu/~sparks/SPICEMODELS.htm](http://www.icaen.uiowa.edu/~sparks/SPICEMODELS.htm))

C) Save the model, complete the circuit & run DC Simulation.
"Pmos transistors:"

There are almost the same as Nmos, however majority carriers are holes ("true" charge) instead of e^-s. Hence, everything is "backward" → we should talk about V_{GS} instead of V_{DS}. In other words, V_{GS}, V_{DS}, V_{TO} & I_{DS} are all negative. Of course, \text{I}_{D}, \text{I}_{P}, K_{P} are positive.

\text{K}_{P} for Pmos is usually half that of an Nmos (since "true" charges move slower than electrons). So, Pmos transistors have usually twice the width of an Nmos for same current drive.
Of course, since I like to avoid negative signs, here are the equations I use for a pmos:

1) Cutoff: \( V_{SG} \leq |V_{TO}| \), \( I_{SD} = 0 \left[ \rho_{pMoS} \right] \)

2) Triode: \( V_{SG} > |V_{TO}| \) \( \Rightarrow I_{SD} = k \left( 2 \left( V_{SG} - |V_{TO}| \right) V_{SD} - V_{S}^2 \right) \)

\( V_{SD} \leq V_{SG} - |V_{TO}| \) \( k = \frac{k_T}{2} \left( \frac{W}{L} \right) \)

3) Saturation: \( V_{SG} \geq |V_{TO}| \) \( \Rightarrow I_{SD} = k \left( V_{SG} - |V_{TO}| \right)^2 \)

\( V_{SD} \geq V_{SG} - |V_{TO}| \)
(a) Find $I_{SS}$

(A') Step (V'): Identify $G$, $D$, $S$ for the PMOS:

Notice how the gate voltage is negative. This makes sense if you look at the semiconductor properties of a PMOS:
(2) Given a mode & solve for $I_{SD}$

Guess relation: $I_{SD} = k (V_{GS} - |V_T|)^2$

Guess solution: $I_{SD} = k (V_{GS} - |V_T|)^2$

\[
\Rightarrow \frac{10 - V_s}{1k} = 2.5 \mu A \frac{V_s}{2}, \quad (2) \left[ (V_s - (2)) - |-0.3| \right]^2
\]

\[
\Rightarrow V_s = 7.76 \text{ V} \quad \text{or} \quad V_s = \nabla \nabla 11.2 \text{ V}
\]

\[V_{TO} = -0.3 \text{ V}\]
\[ V_s = 7.76 \, V \]

Check: Is PMOS on & saturated?

\[ V_{SD} = 7.76 \, V - (-2 \, V) = 9.76 \, V \geq \left[ -0.3 \, V \right] \]

\[ \Rightarrow \text{PMOS on} \]

\[ V_{SD} = V_s - V_D = 7.76 - 0 = 7.76 \, V \leq \frac{9.76 - (-0.3)}{V_{GS}} \]

\[ \Rightarrow \text{oops, PMOS is actually in triode!} \]

Redoing the problem using triode eqn:

\[ I_{SD} = k \left[ \frac{2 (V_{SC} - V_{TO})}{2} \right] \left( V_{SD} - V_{SD^2} \right) \]

\[ \Rightarrow \frac{10 - V_s}{11} = \left( \frac{2 \, k \, V_{TH}^2}{2} \right) \left( \frac{2}{1} \right) \left[ 2 \left( V_s - (-2) - (-0.3) \right) \right] V_s - V_s^2 \]
\[ V_s = 7.81 \text{ V} \quad \text{or} \quad V_s = 5.2 \text{ V} \]

\[ I_{SB} = \frac{10 - 7.8}{10} = 2.19 \text{ mA} \]

Notice how this problem shows the "swept" behaviour of a PMOS compared to an NMOS. We would have expected the PMOS to be in saturation since \( 10 \text{ V} > -2 \text{ V} \). But it is actually in triode!
Note: For simulating pmos in PSPICE, select MbreakP from BREAKOUT and hook up Bulk to Source as shown above. Rest of the steps is the same.