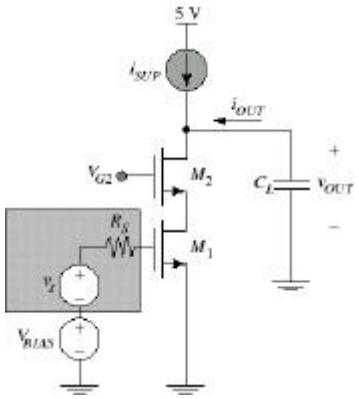
CMOS Cascode Transconductance Amplifier

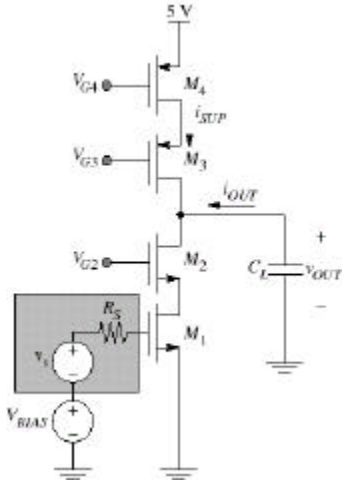
- Basic topology.



- Current supply must have a very high source resistance r_{oc} since otherwise it will limit the output resistance of the amplifier

Current Supply Topology

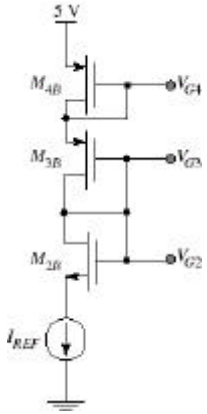
- p-channel cascode current supply is an obvious solution



- need to design a totem pole voltage supply to generate V_{G2}, V_{G3}, and V_{G4}

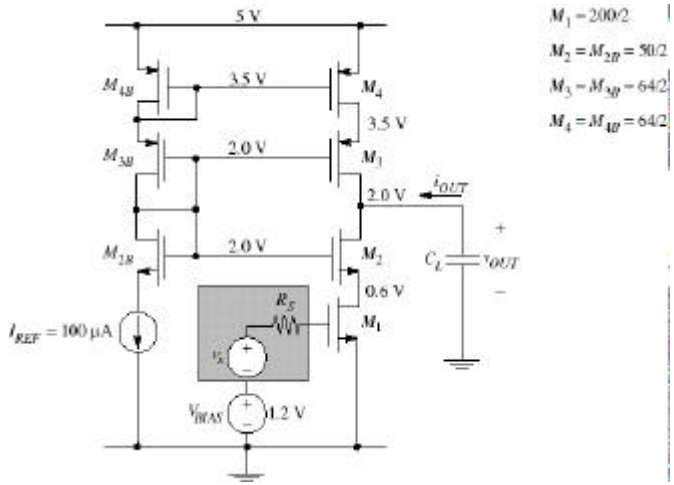
Totem Pole Voltage Reference

- Match device sizes of M_{2B}, M_{3B}, and M_{4B} to M_2, M_3, and M_4



Complete Transconductance Amplifier

- V_{BIAS}: user must supply a *very* precise DC voltage $V_{BIAS} \approx 1.2$ V so that the CS/CG cascode is biased so that it is in the high gain region



CS-CG two-port parameters: $G_m = g_{m1}$

Output resistance: $R_{out} = r_{o2}(1 + g_{m2}\, r_{o1}) \parallel r_{o3}(1 + g_{m3}\, r_{o4})$

Output swing:

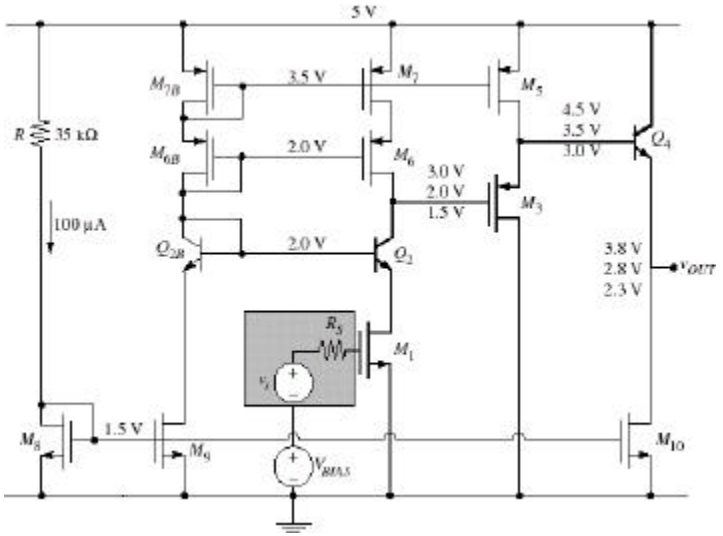
$V_{OUT(max)} = V_{D4} - V_{SD3(sat)} = V_{DD} - V_{SG4B} - V_{SG3B} + V_{SG3} - V_{SD3(sat)}$

$V_{OUT(max)} = 5\text{ V} - 1.5\text{ V} - 1.5\text{ V} + 1.5\text{ V} - 0.5\text{ V} = 3.0\text{ V}$

$V_{OUT(min)} = V_{D1} + V_{DS2(sat)} = V_{G2} - V_{GS2} + V_{DS2(sat)} = 2\text{ V} - 1.4\text{ V} + 0.4\text{ V} = 1\text{ V}$

Multistage Voltage Amplifier

Example to understand a complicated circuit



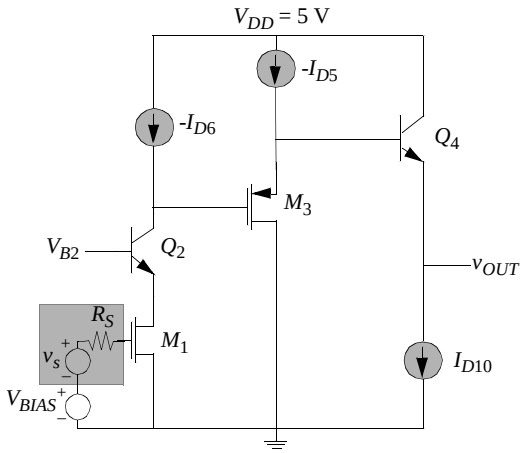
- 10 MOSFETs, 3 BJTs, 1 resistor ... must identify building blocks

  Step-by-step approach to identifying the "important" transistors --

1. replace all transistor current sources and voltage sources by their symbols -- look for diodes and current mirrors! (M_5, M_6/M_{6B}, M_7/M_{7B}, and M_{10} and Q_{2B} are part of current sources or a totem pole voltage reference.)
2. for the (few) remaining transistors, identify the type and use two-port small-signal models to understand the circuit's operation. (For the above amplifier, the remaining transistors are M_1, Q_2, M_3, and Q_4.)

Eliminating Current and Voltage Sources

- Replace current and voltage sources with symbols



Identifying Amplifier Stages

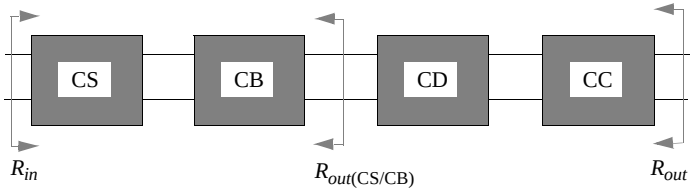
n-channel MOSFET M_1 has its source grounded --> common source

npn BJT Q_2 has its gate tied to a voltage source (from "totem pole" string of diode-connected transistors) --> common base

p-channel MOSFET M_3 has its drain connected to ground --> common drain

npn BJT Q_4 has its collector tied to the positive supply --> common collector

Voltage amplifier is a cascade of two-port models:



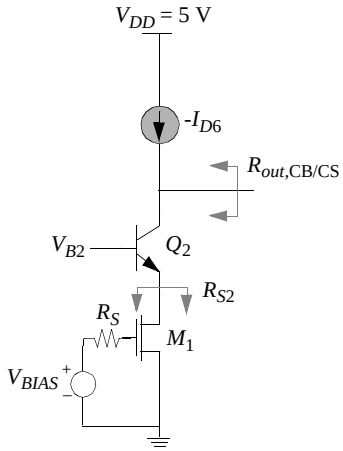
1. common source/common base with cascoded current-source supply: very high output resistance R_{out}(CS/CB) --> can get extremely high output resistance, with a transconductance equal to that of the CS stage

2. common drain: no loading on previous stage since infinite input resistance

3. common collector: low output resistance

Cascode Stage Output Resistance

- Cascode input stage output resistance determines gain



- Output resistance: note that $R_{S2} = r_{o1} >> r_{\pi 2}$

$$R_{out,\mathrm{CB}} = (\beta_{o2} r_{o2}) \| r_{oc6} = (\beta_o r_{o2}) \| (r_{o6}(1 + g_{m6} r_{o7}))$$

CS-CB-CD-CC Two-Port Parameters

- Since CC and CD stages have unity gain (approximately), we can quickly estimate the voltage gain by finding v_{in3}/v_{in} where v_{in3} is the input to the CD stage
- Voltage gain:

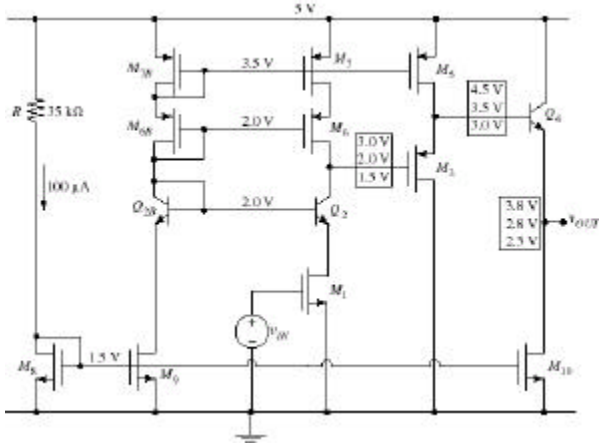
$$A_v \approx (-g_{m1})R_{out,\text{CB}} = -g_{m1}((\beta_o r_{o2}) \| (r_{o6}(1 + g_{m6}r_{o7})))$$

- Output resistance: source resistance of CC output stage is relatively small, since it preceded by a CD stage.

$$R_{out} = R_{out,\text{CC}} \approx \frac{1}{g_{m4}} + \frac{R_{S,\text{CC}}}{\beta_{o4}} = \frac{1}{g_{m4}} + \frac{1}{g_{m3}\beta_{o4}}$$

DC Bias and Output Swing

- Assuming all n-channel devices have V_{GS} = 1.5 V and p-channel devices have V_{SG} = 1.5 V, we can find all the node voltages ... we also assume that V_{BIAS} has been adjusted such that the circuit is in the high-gain region



- Output swing: must consider the limited swing of previous stages (back to cascode) since the the CD/CC output stages are “DC level shifters”

Multistage Amplifier Frequency Response

- Summary of frequency response of single-stages:

  CE/CS: suffers from Miller effect

  CC/CD: "wideband" -- see Section 10.5

  CB/CG: "wideband" -- see Section 10.6

  (wideband means that the stage operates to near the frequency limit of the device ... f_T)

- How to find the Bode plot for a general multistage amplifier?

  can't handle *n* poles and *m* zeroes analytically --> SPICE!

  develop analytical tool for an important special case:

  *** no zeroes**

  *** exactly one "dominant" pole** ($\omega_1 << \omega_2, \omega_3, \ldots, \omega_n$)

$$\frac{V_{out}}{V_{in}} = \frac{A_o}{(1 + j(\omega/\omega_1))(1 + j(\omega/\omega_2))(\ldots)(1 + j(\omega/\omega_n))}$$

(the example shows a voltage gain ... it could be I_{out}/V_{in} or V_{out}/I_{in})

Finding the Dominant Pole

- Multiplying out the denominator:

$$\frac{V_{out}}{V_{in}} = \frac{A_o}{1 + b_1 j\omega + b_2 (j\omega)^2 + \ldots + b_n (j\omega)^n}$$

The coefficient b_1 originates from the sum of $j\omega/\omega_i$ factors --

$$b_1 = \frac{1}{\omega_1} + \frac{1}{\omega_2} + \ldots + \frac{1}{\omega_n} = \sum_i^n \frac{1}{\omega_i} \approx \frac{1}{\omega_1}$$

Therefore, if we can estimate the linear coefficient b_1 in the demoninator polynomial, we can estimate of the dominant pole

Procedure: see P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed., Wiley, 1994, pp. 502-504.

1. Find circuit equations with current sources driving each capacitor
2. Denominator polynomial is determinant of the matrix of coefficients
3. b_1 term comes from a sum of terms, each of which has the form:

$$R_{Tj}\, C_j$$

where C_j is the j^{th} capacitor and R_{Tj} is the Thévenin resistance across the j^{th} capacitor terminals (with all capacitors open-circuited)

Open-Circuit Time Constants

- The dominant pole of the system can be estimated by:

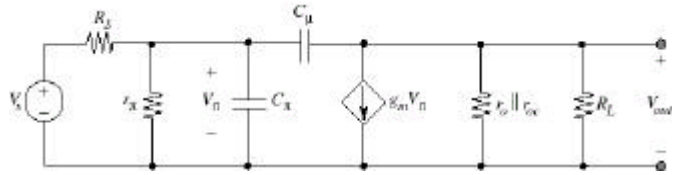
$$\omega_1 \approx \frac{1}{b_1} = \left(\sum_j^n R_{Tj} C_j\right)^{-1} = \left(\sum_1^n \tau_j\right)^{-1},$$

where $\tau_j = R_{Tj}\, C_j$ is the **open-circuit time constant** for capacitor C_j

- This technique is valuable because it estimates the contribution of each capacitor to the dominant pole frequency *separately* ... which enables the designer to understand what part of a complicated circuit is responsible for limiting the bandwidth of the amplifier.

Example: Revisit CE Amplifier

- Small-signal model:



- Apply procedure to each capacitor separately

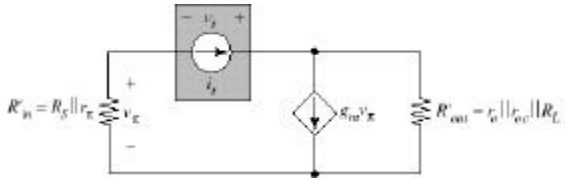
1. C_π's Thévenin resistance is found by inspection as the resistance across its terminals with all capacitors open-circuited:

$$R_{T\pi} = R_S \| r_\pi = R_{in}' \dashrightarrow \tau_{C_{\pi o}} = R_{T\pi} C_\pi$$

2. C_μ's Thévenin resistance is *not* obvious --> must use test source and network analysis

Time Constant for C_μ

- Circuit for finding $R_{T\mu}$



v_π is given by:

$$v_\pi = -i_t(R_s \| r_\pi) = -i_t R_{in}'$$

v_o is given by:

$$v_o = -i_o R_{out}' = (i_t - g_m v_\pi) R_{out}' = i_t(g_m R_{in}' + 1) R_{out}'$$

v_t is given by:

$$v_t = v_o - v_\pi = i_t((1 + g_m R_{in}') R_{out}' + R_{in}')$$

solving for $R_{T\mu} = v_t / i_t$

$$R_{T\mu} = R_{in}' + R_{out}' + g_m R_{in}' R_{out}'$$

$$\boxed{\tau_{C_{\mu o}} = R_{T\mu} C_\mu = (R_{in}' + R_{out}' + g_m R_{in}' R_{out}') C_\mu}$$

Estimate of Dominant Pole for CE Amplifier

- Estimate dominant pole as inverse of sum of open-circuit time constants

$$\omega_1^{-1} = (R_{T\pi} C_\pi + R_{T\mu} C_\mu) = R_{in}' C_\pi + (R_{in}' + R_{out}' + g_m R_{in}' R_{out}') C_\mu$$

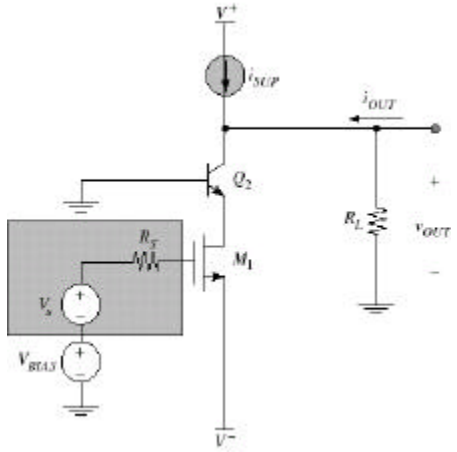
inspection --> identical to "exact" analysis (which also assumed $\omega_1 \ll \omega_2$)

- Advantage of open-circuit time constants: *general* technique

Example: include C_{cs} and estimate its effect on ω_1

Multistage Amplifier Frequency Response

- Applying the open-circuit time constant technique to find the dominant pole frequency -- use CS/CB cascode as an example

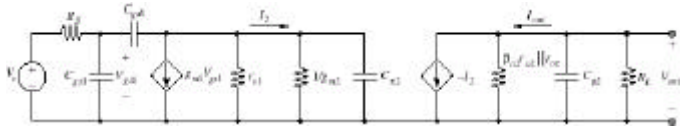


- Systematic approach:

  1. two-port small-signal models for each stage (*not* the device models!)
  2. carefully add capacitances across the appropriate nodes of two-port models, which may not correspond to the familiar device configuation for some models

Two-Port Model for Cascode

- The base-collector capacitor $C_{\mu 2}$ is located between the output of the CB stage (the collector of Q_2) and small-signal ground (the base of Q_2)



We have omitted C_{db1}, which would be in parallel with $C_{\pi 2}$ at the output of the CS stage, and C_{cs2} which would be in parallel with $C_{\mu 2}$. In addition, the current supply transistor will contribute additional capacitance to the output node.

- Time constants

$$\tau_{C_{gs1o}} = R_S C_{gs1}$$

$$\tau_{C_{gd1o}} = (R_{in}' + R_{out}' + g_{m1} R_{in}' R_{out}') C_{gd1}$$

where $R_{in}' = R_S$ and $R_{out}' = r_{o1} \| \left(\frac{1}{g_{m2}} \right) \approx \frac{1}{g_{m2}}$

Since the output resistance is only $1/g_{m2}$, the Thévenin resistance for C_{gd1} is not magnified (i.e., the Miller effect is minimal):

$$\tau_{C_{gd1o}} = \left(R_S + \frac{1}{g_{m2}} + \left(\frac{g_{m1}}{g_{m2}} \right) R_S \right) C_{gd1} \approx R_S (1 + g_{m1}/g_{m2}) C_{gd1}$$

Cascode Frequency Response (cont.)

- The base-emitter capacitor of Q_2 has a time constant of

$$\tau_{C_{\pi 2o}} = \left(\frac{1}{g_{m2}}\right) C_{\pi 2}$$

- The base-collector capacitor of Q_2 has a time constant of

$$\tau_{C_{\mu 2o}} = (\beta_{o2} r_{o2} \| r_{oc} \| R_L) C_{\mu 2} \approx R_L C_{\mu 2}$$

- Applying the theorem, the dominant pole of the cascode is approximately

$$\omega_{3db}^{-1} \approx \tau_{C_{gs1o}} + \tau_{C_{gd1o}} + \tau_{C_{\pi 2o}} + \tau_{C_{\mu 2o}}$$

$$\omega_{3db}^{-1} \approx R_S C_{gs1} + R_S(1 + g_{m1}/g_{m2}) C_{gd1} + \left(\frac{1}{g_{m2}}\right) C_{\pi 2} + R_L C_{\mu 2}$$

Gain-Bandwidth Product

- A useful metric of an amplifier's frequency response is the product of the low-frequency gain $|A_{vo}|$ and the 3 dB frequency ω_{3dB}

  For the cascode, the gain is $|A_{vo}| = |-g_{m1}R_L|$ and the gain-bandwidth product is

$$|A_{vo}|\omega_{3dB} \approx \frac{g_{m1} R_L}{R_S C_{gs1} + R_S(1 + g_{m1}/g_{m2}) C_{gd1} + \left(\frac{1}{g_{m2}}\right) C_{\pi 2} + R_L C_{\mu 2}}$$

- If the voltage source resistance is small, then

$$|A_{vo}|\omega_{3dB} \approx \frac{g_{m1} R_L}{(C_{\pi 2}/g_{m2} + R_L C_{\mu 2})}$$

  which has the same form as the common-base gain-bandwidth product (and which is *much* greater than the Miller-degraded common-source)