Depletion Capacitance

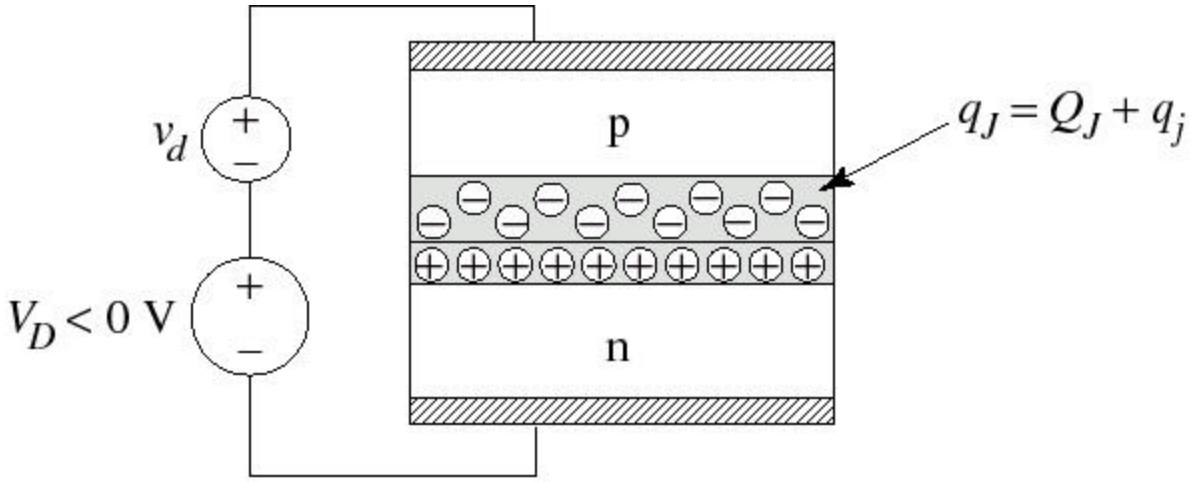
Basic circuits: $Q = C\,V$ ... linear capacitor

Semiconductor devices: non-linear charge storage elements (e.g., the depletion region in a pn junction under reverse bias)

What do we do with $Q = f(V)$? Linearize it ... for small variations in V

**** *WARNING:* DECEPTIVELY DIFFICULT CONCEPT ****

$C_j = dq / dv$ ... **incremental** charge-storage capacitance is defined as a *small signal* quantity. The derivative is evaluated at a particular DC diode voltage V_D



- break up the total applied voltage (symbol: v_D) into two parts:

total voltage = DC voltage + small-signal voltage

$$v_D = V_D + v_d$$

Depletion Capacitance (cont.)

- break up the charge q_J on the p-side of the junction similarly:

  total charge in the depletion region = DC charge + small-signal charge

  $$q_J = Q_J + q_j$$

  note that the DC charge is a negative number

- Since the incremental charge q_j and the incremental voltage are "small" (define what small means later),

  $$q_j \propto v_d$$

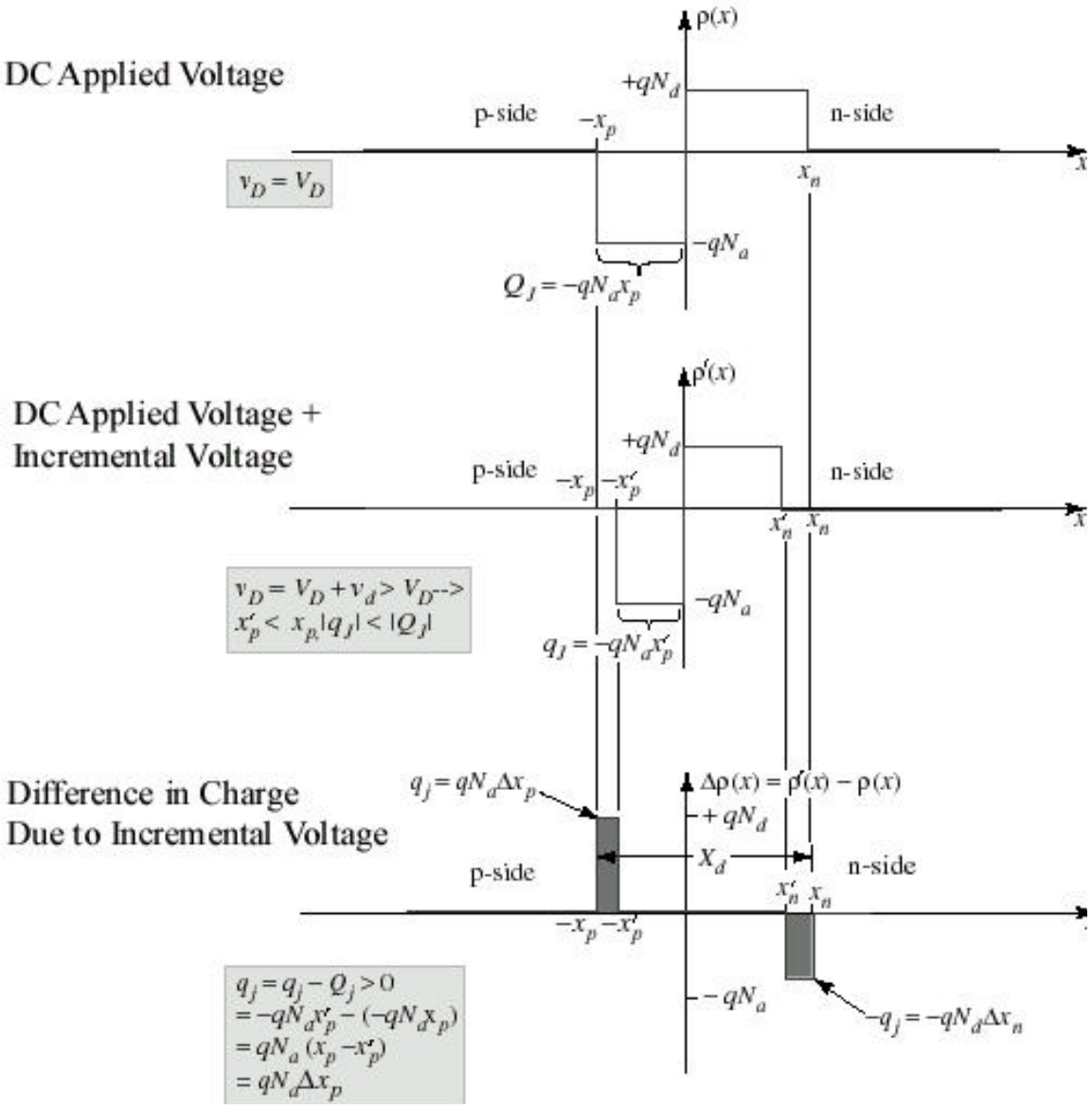
  the proportionality constant has units of capacitance [F] or more commonly capacitance per unit area [F/cm^2] -- since the charge is in C/cm^2

- Define the junction capacitance C_j as the proportionality constant

  $$C_j = \frac{q_j}{v_d} = \frac{\Delta q_J}{\Delta v_D}$$

Depletion Capacitance: Physical Interpretation

Look at the difference in the depletion charge due to the incremental voltage



The difference in charge is separated by the DC depletion width (approximately) ... just a parallel plate capacitor!

Depletion Capacitance Equation

- The incremental charge is two sheets separated by a distance $X_d(V_D)$ ... where the ( ) indicate the functional dependence.
- Use the parallel plate capacitor formula from Physics 7B:

$$C_j = \frac{\varepsilon_s}{X_d(V_D)} = \frac{\varepsilon_s}{X_{do}\sqrt{1 - V_D/\phi_B}} = \frac{C_{jo}}{\sqrt{1 - V_D/\phi_B}} \text{ (per unit area)}$$

- Alternative approach for those who prefer math to physics:

$$C_j = \left.\frac{\Delta q_J}{\Delta v_D}\right|_{V_D} = \left.\frac{dq_J}{dv_D}\right|_{V_D}$$

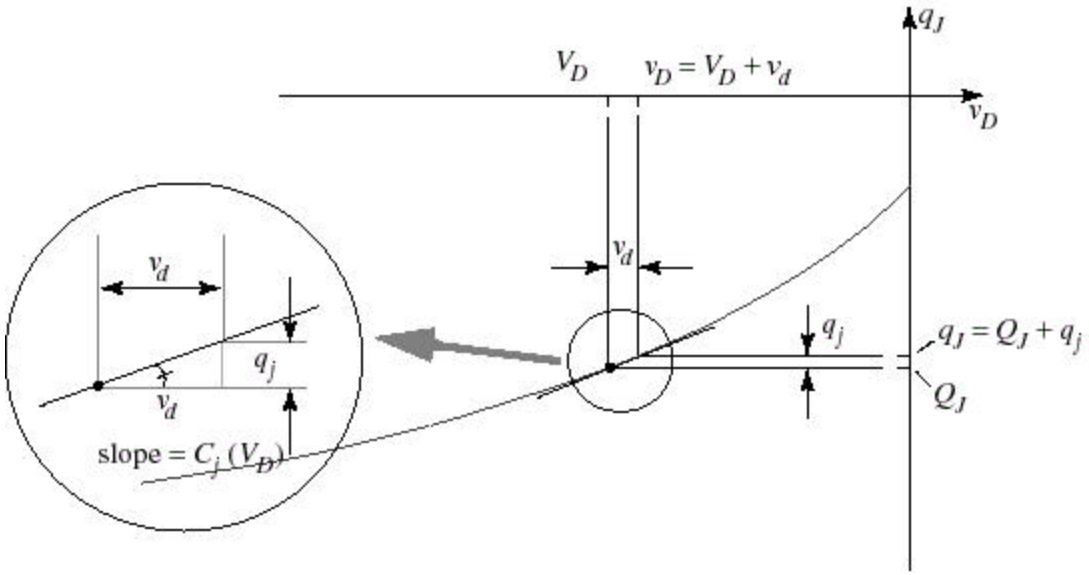
- Find the depletion charge (on the p-side) $q_J = q_J(v_D)$ from $x_p(v_D)$ and differentiate

$$q_J(v_D) = -qN_a x_p(v_D) = -qN_a x_{po}\sqrt{1 - (V_D + v_d)/\phi_B}$$

- To find the depletion capacitance C_j we simply take the derivative and evaluate it at the particular DC voltage

Graphical Interpretation

- Derivative is the *slope* of the plot of $q_J(V_D)$:



Note that C_j (the slope) is clearly a function of dc bias V_D

- Some observations:

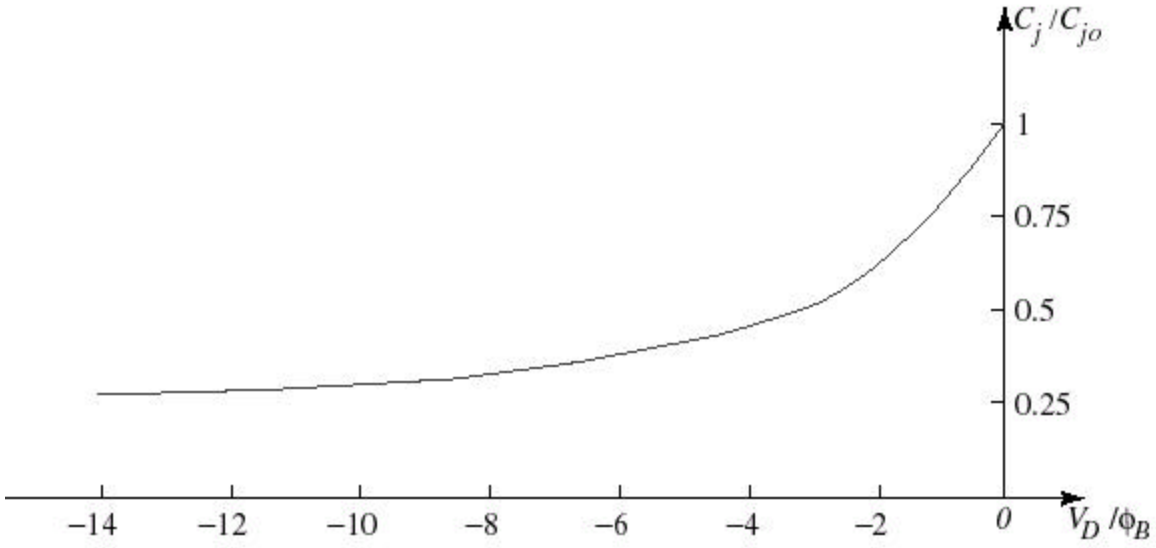
1. The ratios q_J / v_D or Q_J / V_D **<u>are not</u>** equal to the capacitance whereas

the ratio q_j / v_d **<u>is</u>** equal to the capacitance! Understand why!

2. If you want a small value for the capacitance, you should apply a larger reverse bias (more negative V_D) to the pn junction.

Depletion Capacitance Numbers

- Plot of depletion capacitance (normalized to C_{jo}):



Typical numbers: Suppose $X_{do} = 0.4\ \mu m$

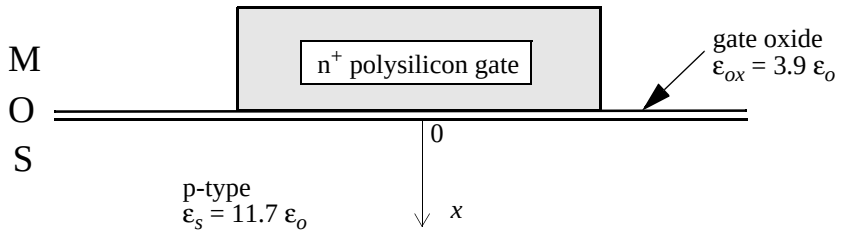
$$C_{jo} = \frac{11.7 \times 8.85 \times 10^{-14} \text{f/cm}}{0.4 \times 10^{-4}} \frac{\text{f/cm}}{\text{cm}} = 2.6 \times 10^{-8} \text{F/cm}^2 = 0.26\ \text{fF}/\mu\text{m}^2$$

With bias: $\phi_B = 0.8$ V --> $V_D = -6.4$ V = $-8\ \phi_B$ then

$$(1 - V_D/\phi_B)^{1/2} = 3 \rightarrow C_j = C_{jo}/3 = 0.086 \frac{\text{fF}}{\mu\text{m}^2} = 86\ \text{aF}/\mu\text{m}^2$$

How much area to get 1 pF?

The MOS Capacitor



Oxide = SiO_2 ... a near-perfect insulator. We assume zero charge inside the oxide for this course

n^+ polysilicon has a potential which is the maximum possible in silicon:

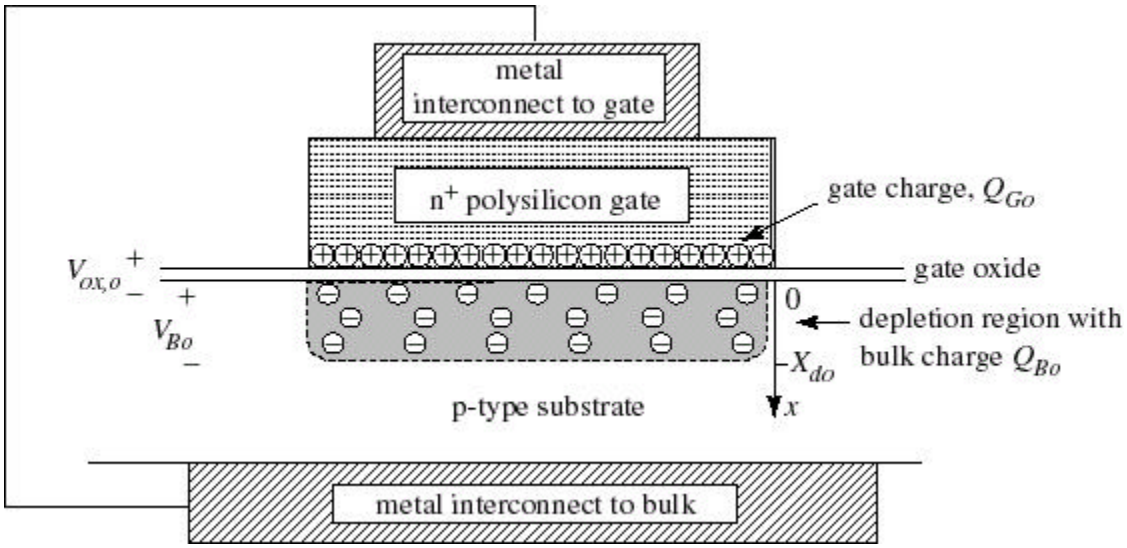
$$\phi_{n+} = 550 \text{ mV}$$

p-type substrate has potential which is $\phi_p = -60 \text{ mV} \log (N_a / 10^{10})$

Thus, there is a *built-in voltage* given by $0.55 + \phi_p$

Qualitative Charge Distribution in Thermal Equilibrium

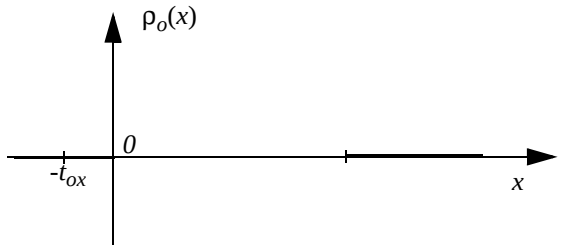
- Where to start: potential in n^+ polysilicon is known; potential in p-type substrate is known, too ... need + charge on gate, - charge in substrate
- since the silicon is p-type, this means that a depletion region (to get the needed negative charge) forms under the gate



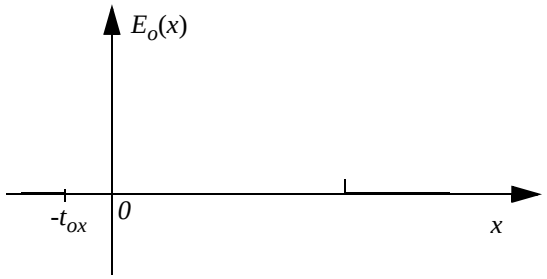
Thermal Equilibrium MOS Electrostatics

- Sketch charge density, electric field, and potential in equilibrium

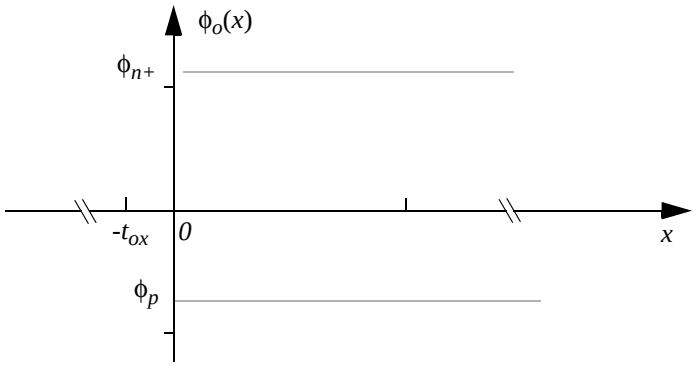
charge density



electric field



potential

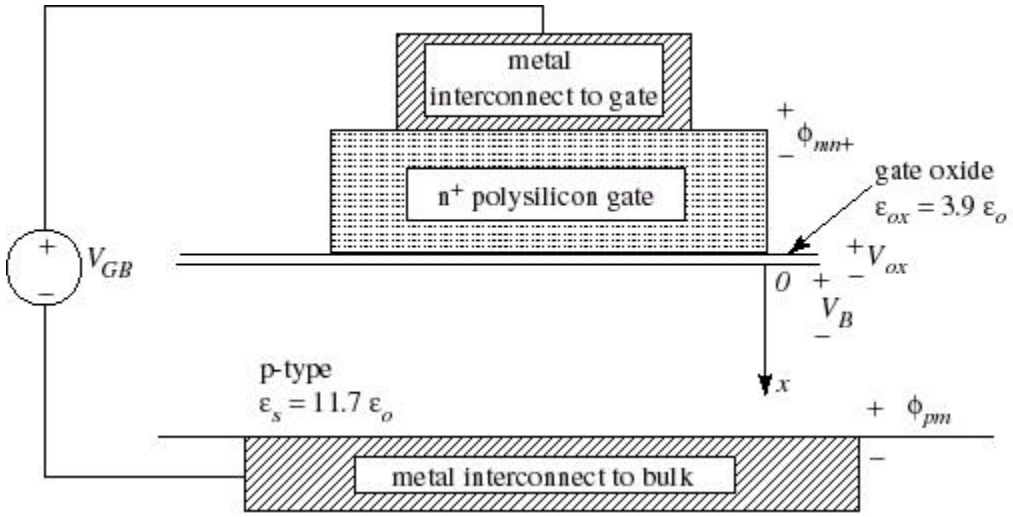


MOS Capacitor under Applied Bias

- Oxide doesn't permit any steady-state current between the n^+ poly gate and the substrate. Therefore, if we wait long enough for transient currents to die out, the electron and hole currents are zero --

$$J_n = 0 \qquad \text{and} \qquad J_p = 0$$

- Even though the structure isn't in equilibrium, the absence of current implies that we can relate potential to carrier concentration in the silicon substrate (since that's all we assumed in deriving the 60 mV rule.)

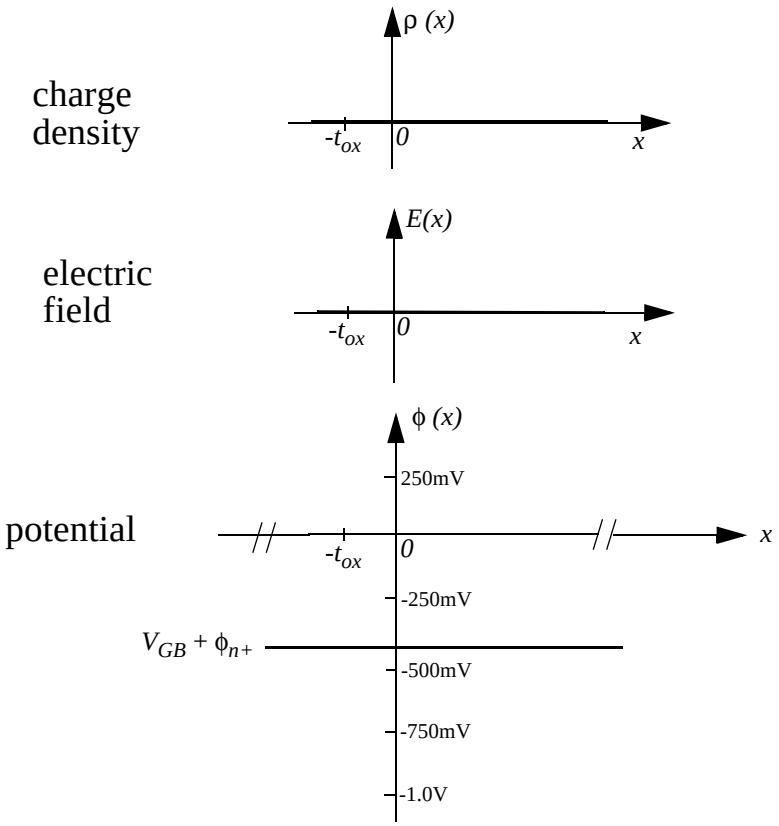


- *Flatband condition*: cancel built-in drop by applying the *flatband voltage*

$$V_{GB} = -(\phi_{n+} - \phi_p) = V_{FB} = -970 \text{ mV for } N_a = 10^{17} \text{ cm}^{-3}$$

MOS Electrostatics in Flatband

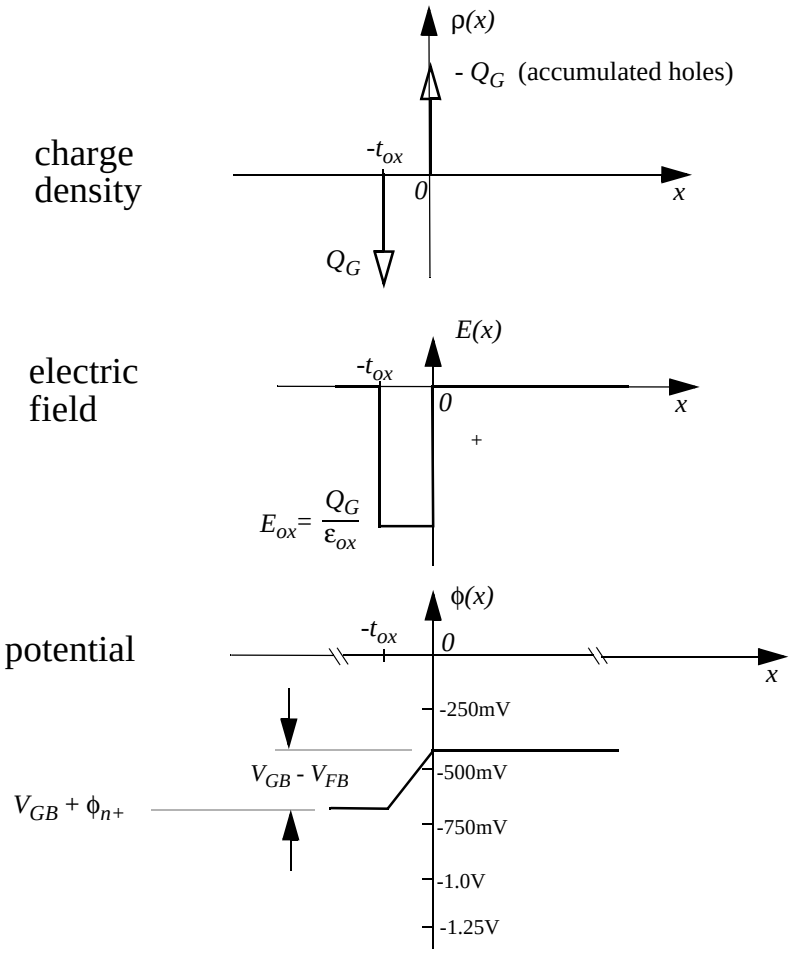
- When $V_{GB} = V_{FB}$, the gate is shifted from its thermal equilibrium potential (ϕ_{n+}) to a new value of $V_{FB} + \phi_{n+} = -(\phi_{n+} - \phi_p) + \phi_{n+} = \phi_p$, which is the same potential as the p-type bulk. Therefore, there is no potential drop across the MOS structure in flatband



- If we continue to make the gate-bulk voltage more negative, the gate will take on a negative charge $Q_G < 0$. The substrate has a positive charge, which comes from holes that are attracted by the negative gate charge

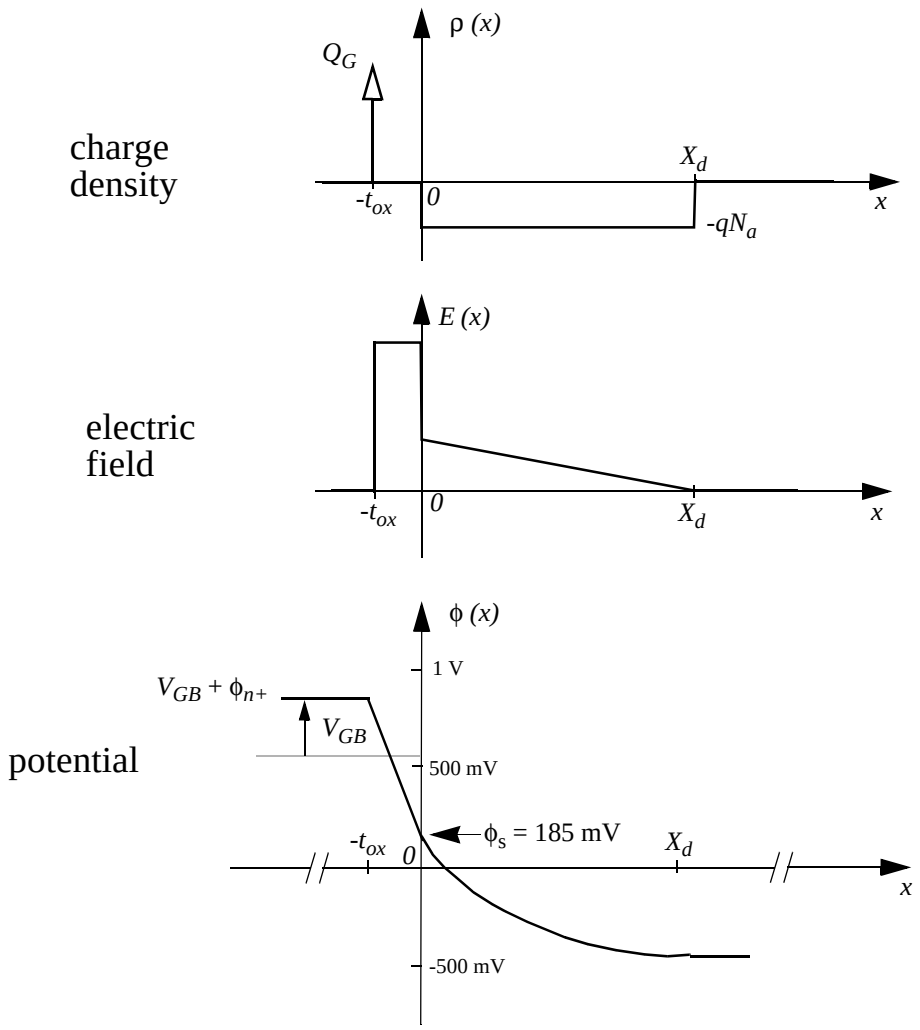
MOS Capacitor in Accumulation

- Charge density, electric field, and potential in accumulation: $V_{GB} < V_{FB}$, where V_{FB} = - 0.97 V for this example.



MOS Capacitor in Depletion

- Now we make $V_{GB} > V_{FB}$. Note that thermal equilibrium falls into this range of applied bias.



- Surface potential at oxide/silicon interface is now positive --> n-type (slightly, $n_s = 10^{13}$ cm^{-3}).

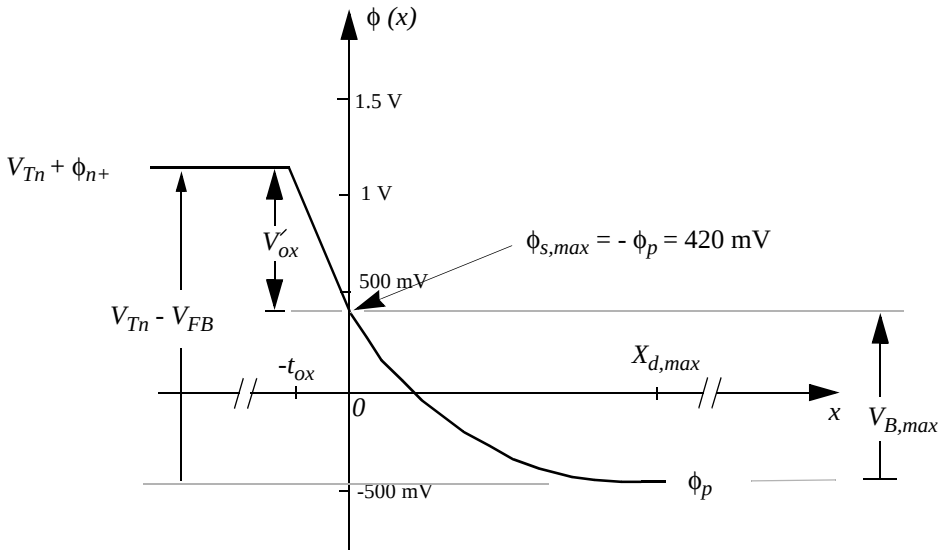
The Threshold Voltage V_{Tn}

- Keep increasing V_{GB}: surface potential keeps increasing. At some point, the surface is n-type (i.e., we say that it is *inverted*) and the electron charge makes a significant contribution to the charge density.

  How do we model this phenomenon? We approximate that onset of inversion as the point where the electron concentration n_s at the surface is the same as the hole concentration N_a in the bulk. (In other words, "the surface is as n-type as the bulk is p-type.")

  The gate-bulk potential at the onset of inversion is called the *threshold voltage*, V_{Tn}. To find the threshold voltage, we need to consider the electrostatics in depletion (no electrons at the surface at the onset of inversion) -- with the surface potential equal to the opposite of the bulk potential:

$$\phi_{s,\,max} = -\phi_p$$



Threshold Voltage Expression

- We can solve for the threshold voltage:

$$V_T - V_{FB} = V_{ox}' + V_{B,\,max}$$

- The drop across the depletion region is

$$V_{B,\,max} = \phi_{s,\,max} - \phi_p = -\phi_p - \phi_p = -2\phi_p$$

- The drop across the oxide for $V_{GB} = V_{Tn}$ is

$$V_{ox}' = E_{ox}' t_{ox} = \left(\frac{-Q_{B,\,max}}{\varepsilon_{ox}}\right) t_{ox} = \frac{-Q_{B,\,max}}{C_{ox}}$$

- The bulk charge in inversion is found from the depletion width $X_{d,max}$

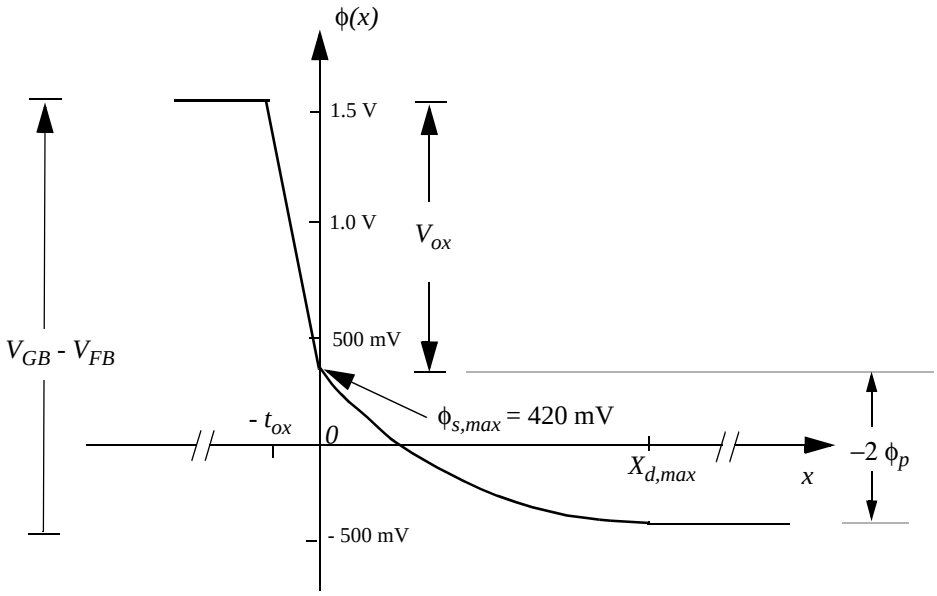
$$Q_{B,\,max} = -qN_a X_{d,\,max} = -qN_a \sqrt{\frac{-2\phi_p}{((1/2)qN_a)/\varepsilon_s}} = -\sqrt{2q\varepsilon_s N_a(-2\phi_p)}$$

where the relationship between the depletion width $X_{d,max}$ and the drop across the depletion region $\phi_{s,max}$ - (ϕ_p) = -ϕ_p - ϕ_p = -2ϕ_p can be found from Poisson's Equation.

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a(-2\phi_p)}$$

The Inverted MOS Capacitor ($V_{GB} > V_{Tn}$)

- We consider the surface potential as fixed ("pinned") at $\phi_{s,max} = -2\,\phi_p$



- What is the inversion charge Q_N?

  Consider: bulk charge is constant for $V_{GB} > V_{Tn}$ so *all* of the additional charge in the silicon is stored in the inversion layer, once inversion occurs.

  The inversion layer is separated from the gate by the gate oxide; we can relate the inversion charge (per cm^2) to the applied voltage over V_{Tn} through C_{ox} the capacitance (per cm^2) of the oxide

$$Q_N = -C_{ox}(V_{GB} - V_{Tn})$$

Charge Storage in the MOS Structure

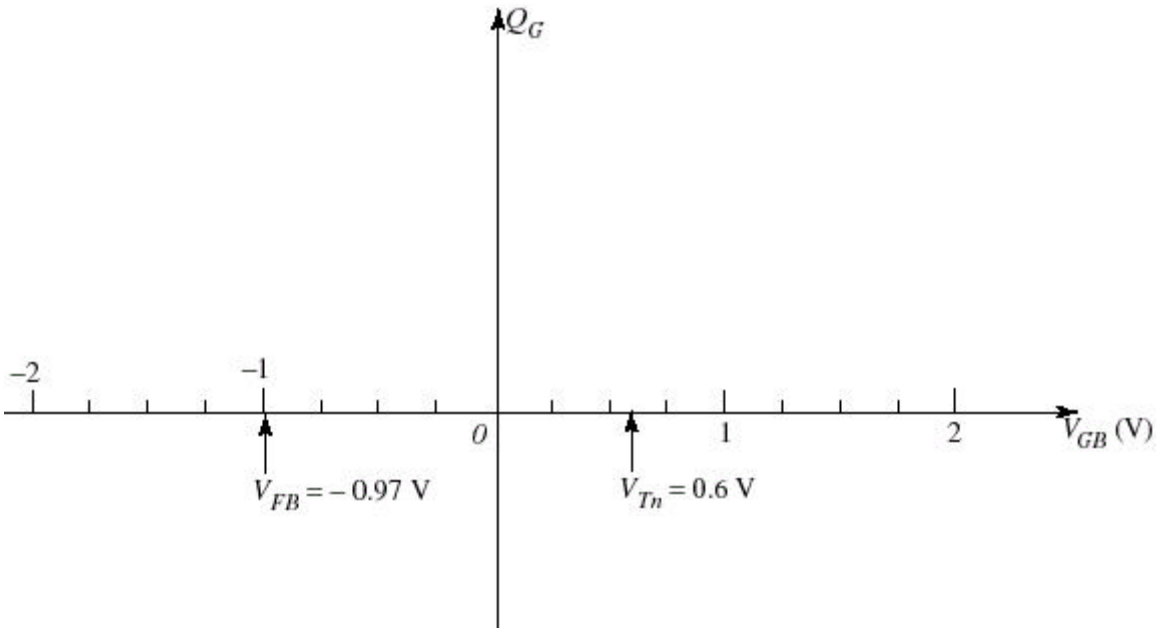
- Three regions of operation:

  Accumulation: $q_G = C_{ox}\,(v_{GB} - v_{FB})$ ... parallel plate capacitor

  Depletion: $q_G = -\,q_B(v_{GB})$, with the bulk (depletion) charge in the silicon being a nonlinear function of v_{GB}

  Inversion: $q_G = -\,q_N - q_{B,max}$, where $q_{B,max} = q_B(v_{GB} = V_T)$ is the depletion charge at the onset of inversion and

- Sketch of the gate charge as a function of gate-bulk voltage:



Understanding MOS Capacitors

- Start with the built-in offset: find the flatband voltage V_{FB}

- Start first with V_{GB} increasing above V_{FB}

  + charge on gate (*why*?)

  - charge in silicon ... decide whether excess electrons (accumulation) or ionized acceptors (depletion) depending on whether silicon substrate is n-type or p-type

- Now decrease V_{GB} below V_{FB}

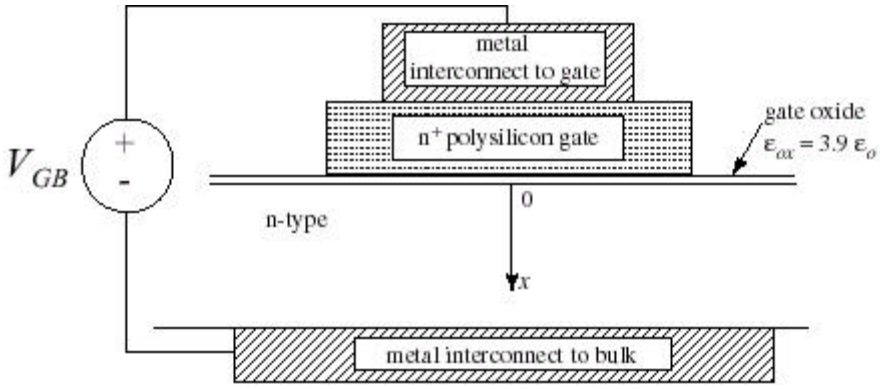
  - charge on gate (*why*?)

  + charge in silicon ... decide whether excess holes (accumulation) or ionized donors (depletion) depending on whether silicon substrate is p-type or n-type

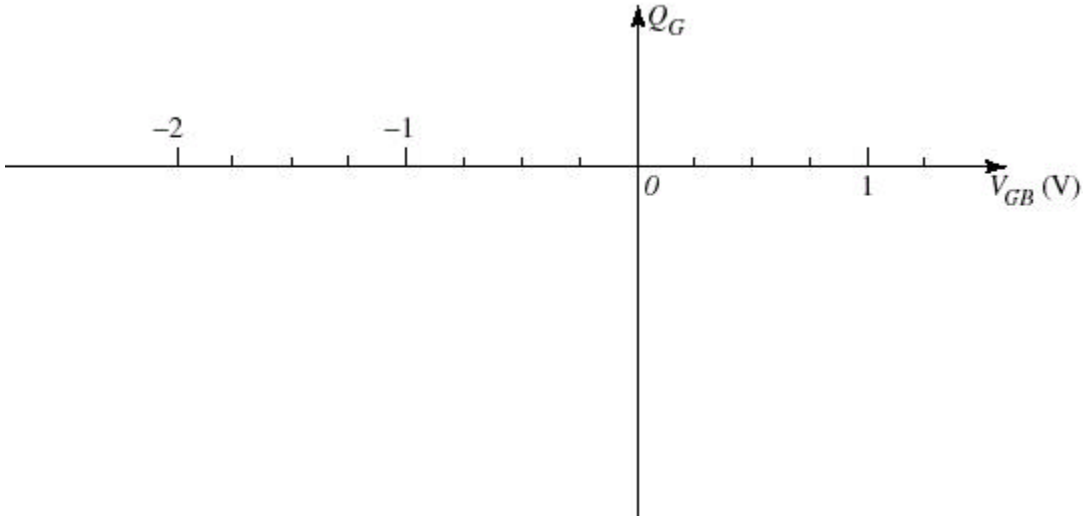
- Inversion occurs “after” depletion; additional data point is state in equilibrium

MOS Capacitor with n-type Silicon

- Structure: gate could be n^+ polysilicon or p^+ polysilicon ... or a metal



- Charge vs. gate-bulk voltage plot

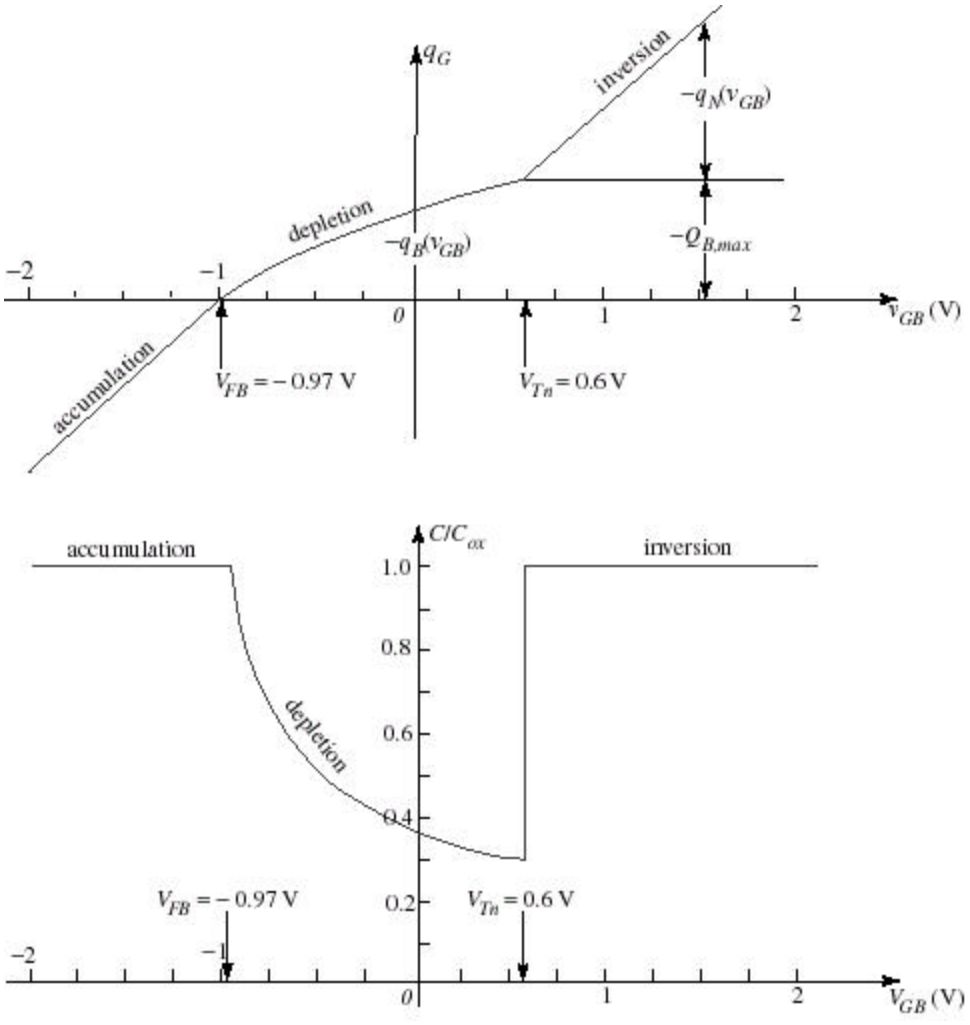


MOS Capacitance

- The capacitance of the MOS structure is defined as

$$C = \left.\frac{dq_G}{dv_{GB}}\right|_{V_{GB}}$$

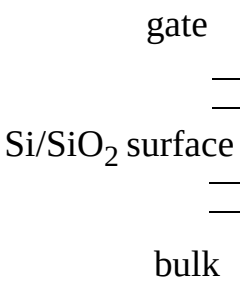
- Could find functional dependence $q_G(v_{GB})$ and evaluate the derivatives ... tough!



Physical Interpretation of MOS Capacitance

- ***Accumulation***: parallel plate capacitor: $C = C_{ox}$

- ***Depletion***: increment in gate charge is mirrored at bottom of depletion region, so capacitance model is C_{ox} in series with the depletion region capacitance C_b



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_b = \frac{\varepsilon_s}{X_d}$$

Note that X_d is a function of V_{GB}

C = C_{ox} in series with C_b

$$C = \frac{\frac{\varepsilon_{ox}}{t_{ox}} \times \frac{\varepsilon_s}{X_d}}{\frac{\varepsilon_{ox}}{t_{ox}} + \frac{\varepsilon_s}{X_d}} =$$

- ***Inversion***: bulk charge is no longer changing with V_{GB}: an increment in gate charge is mirrored in the inversion layer under the gate.

  That is, $\delta Q_{\underset{+\text{ charge}}{\text{gate}}} = \delta Q_{\underset{\text{electrons}}{\text{surface}}}$

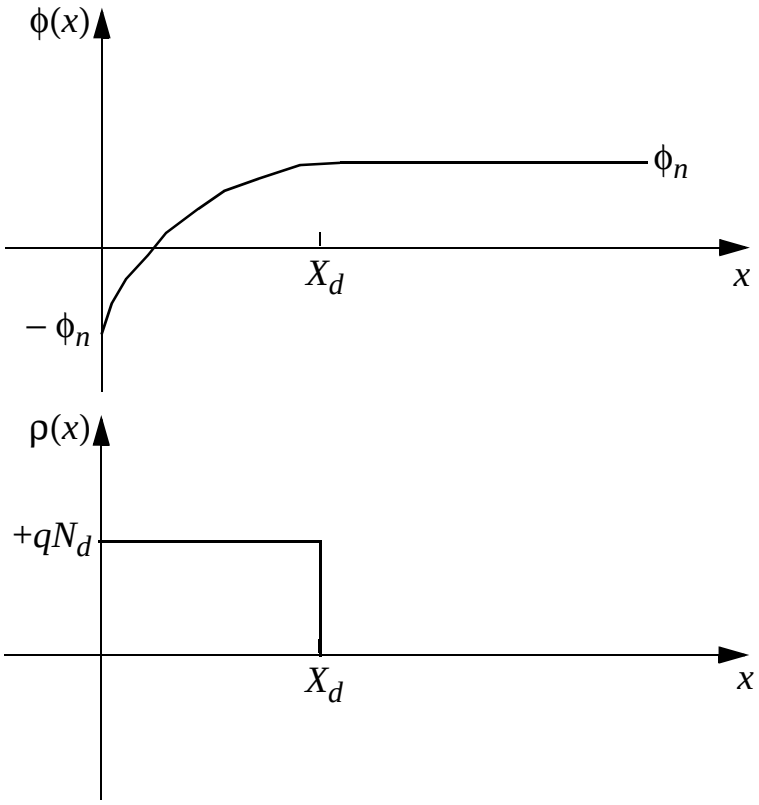
  The capacitance is therefore the same as in accumulation: $C = C_{ox}$

MOS *C-V* Curves

- construct $C(V_{GB})$ plot based on knowledge of state of the MOS capacitor, along with the values of V_{FB}, V_T, C_{ox}, and the minimum capacitance C_{min}

- The minimum capacitance occurs just prior to inversion, so the surface potential is opposite of the bulk potential

  drop across depletion region is therefore $2\phi_n$ (for n-type substrate case)



MOS Capacitance-Voltage Curve (Cont.)

- Maximum depletion width can be found by integrating the charge density twice:

$$2\phi_n = \int_0^X \left[\int_0^x \frac{\rho(x)}{\varepsilon_s} dx \right] dx = \int_0^X \left[\int_0^x \frac{q\mathrm{Nd}}{\varepsilon_s} dx \right] dx = \left(\frac{1}{2}\right)\left(\frac{qN_d}{\varepsilon_s}\right) X_{d,\,max}^2$$

$$C_{min} = \left(\frac{\varepsilon_{ox}}{t_{ox}}\right) \Big\| \left(\frac{\varepsilon_s}{X_{d,\,max}}\right)$$

- Sketch the *normalized* capacitance curve knowing V_{FB}, V_T, C_{ox}, and C_{min}