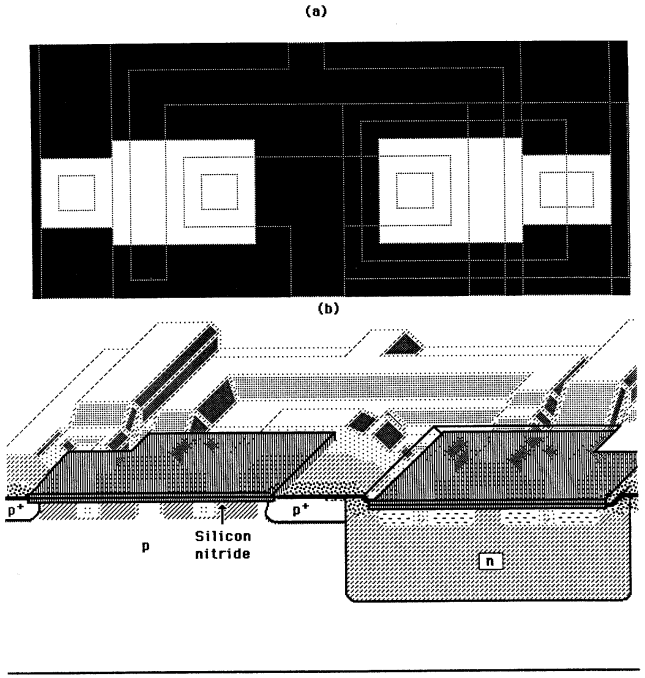

Figure 5-2: Formation of the active regions in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

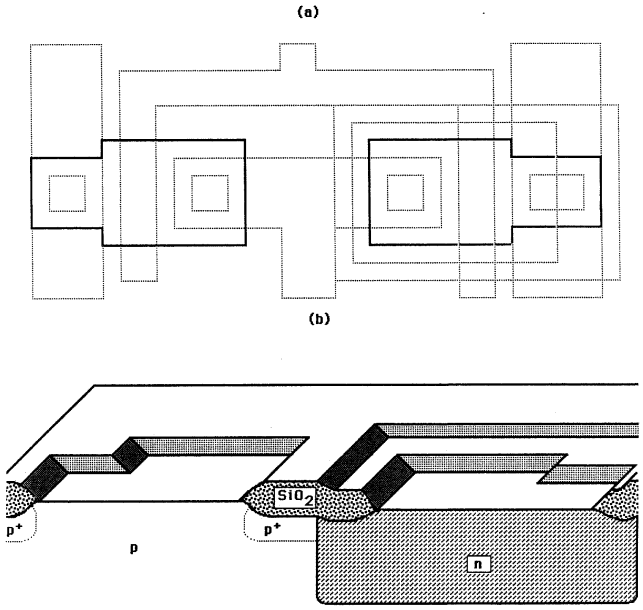

Figure 5-3: Active regions in the n-well CMOS inverter. Edges of active regions in the mask (a) and cross-section of the inverter (b).

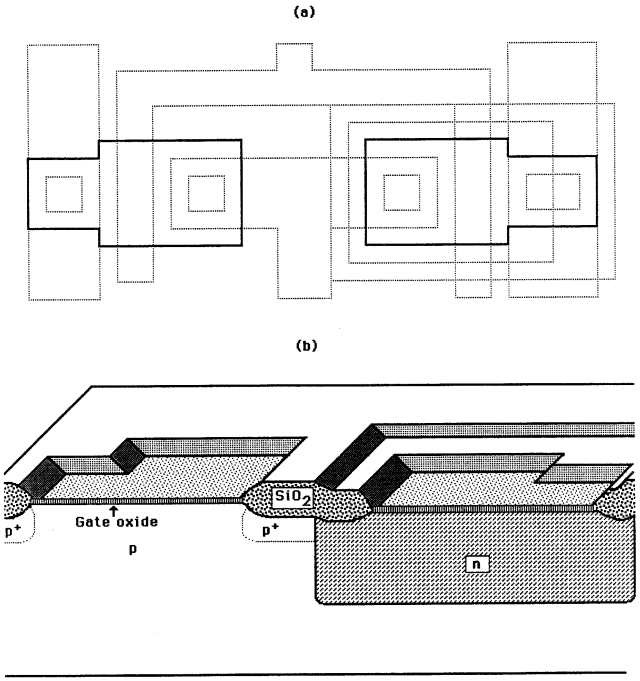

Figure 5-4: Gate oxide growth in the n-well CMOS inverter. Edges of the gate oxide regions (a) and cross-section of the inverter (b).

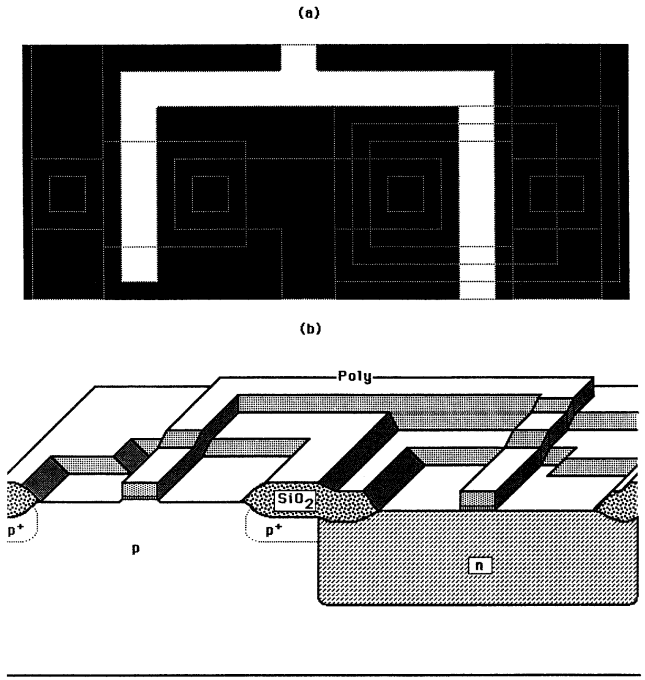

Figure 5-5: Polysilicon region in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

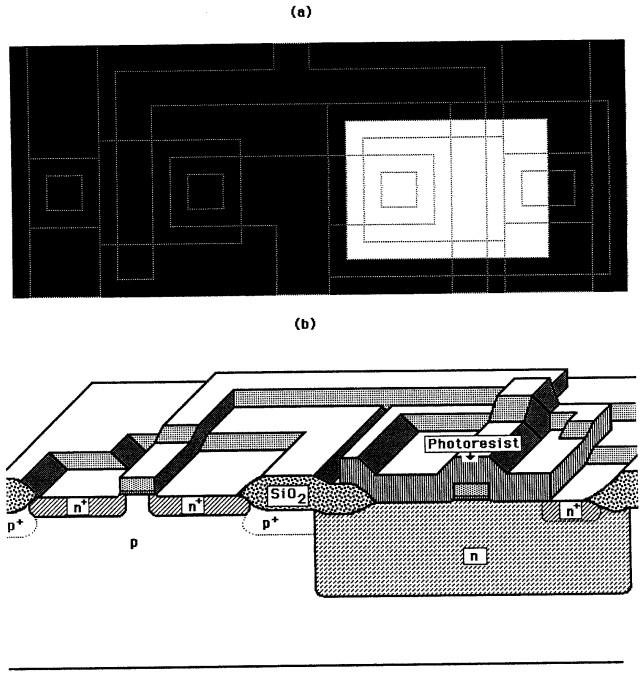

Figure 5-6: Implantation of n-channel transistor drain and source. Window in the n-select mask (a) and cross-section of the inverter (b).

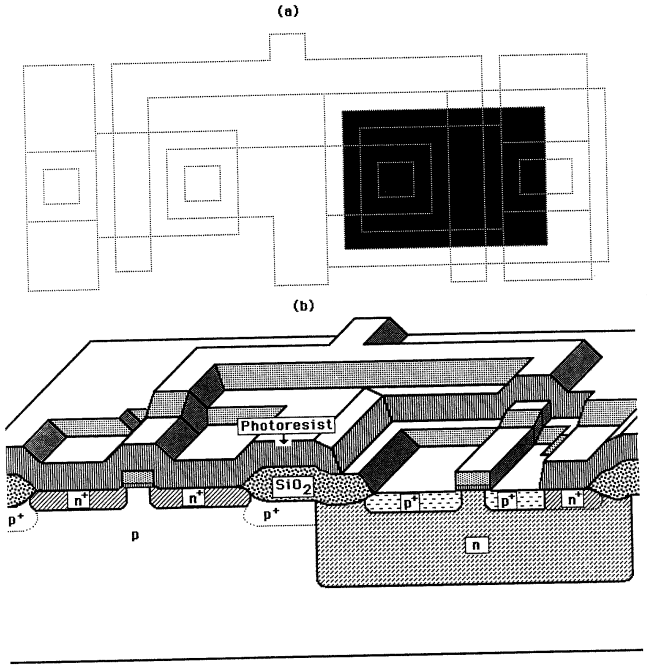

Figure 5-7: Implantation of p^+ regions. Window in the negative of the n-select mask (a) and cross-section of the inverter (b).

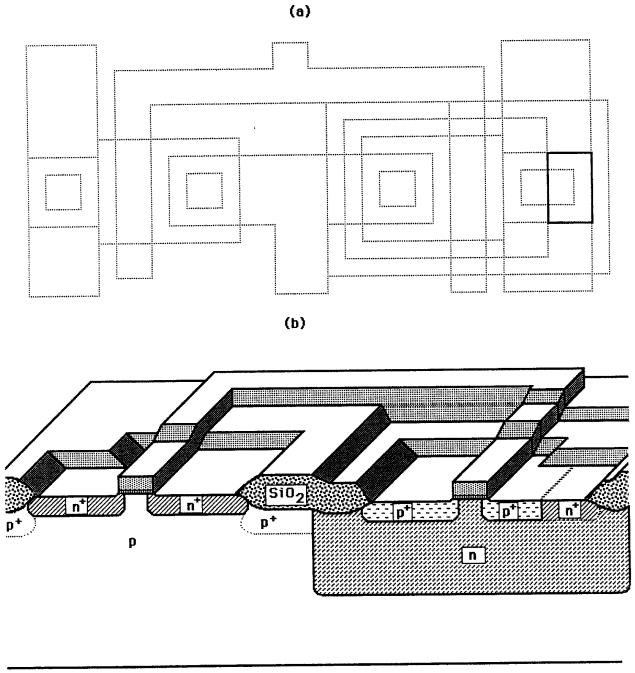

Figure 5-8: N^+ region in the n-well of the CMOS inverter. Edges of the drain region of the p-channel device and the n^+ region in the n-well (a) and cross-section of the inverter (b).

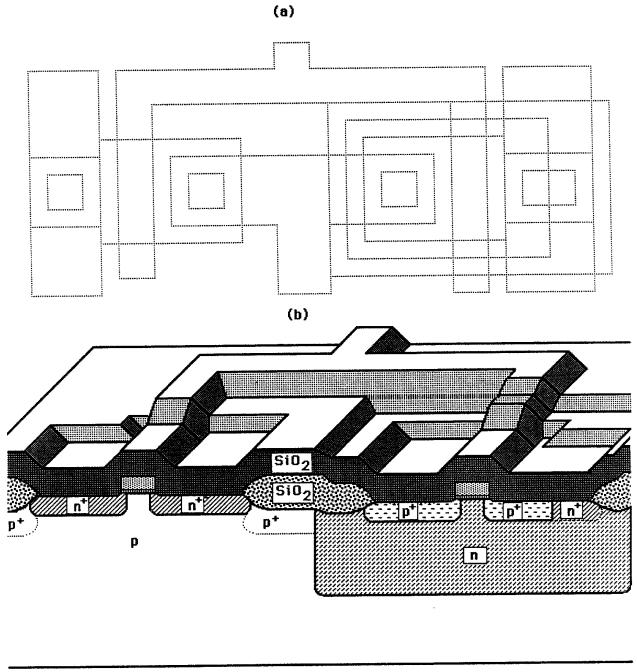

Figure 5-9: CVD deposition of SiO_2 in the n-well CMOS process. Layout (a) and cross-section of the inverter (b).

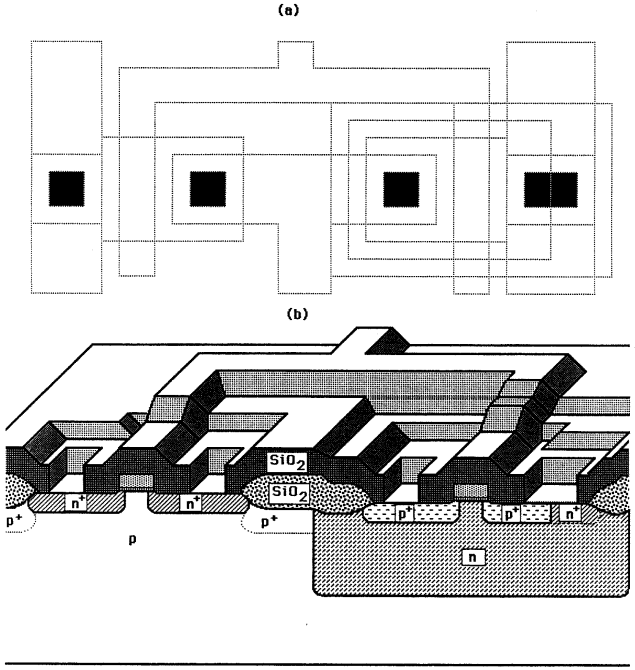

Figure 5-10: Contact cuts in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

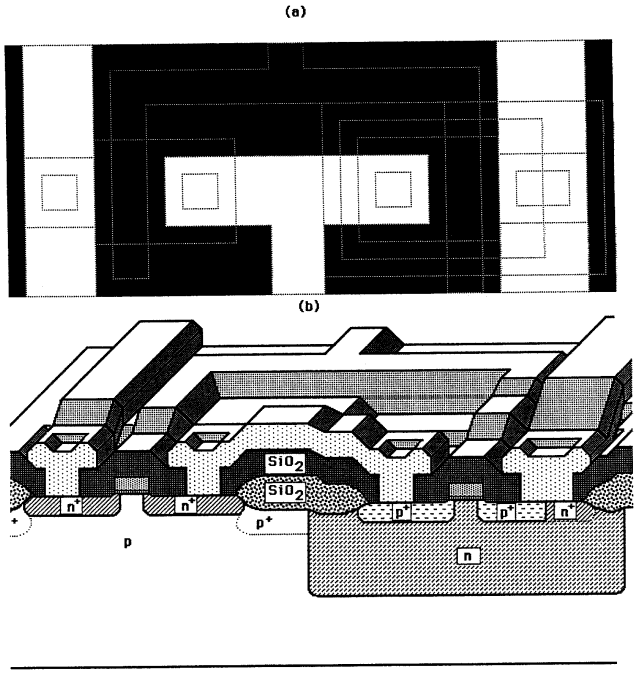

Figure 5-11: Metallization in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

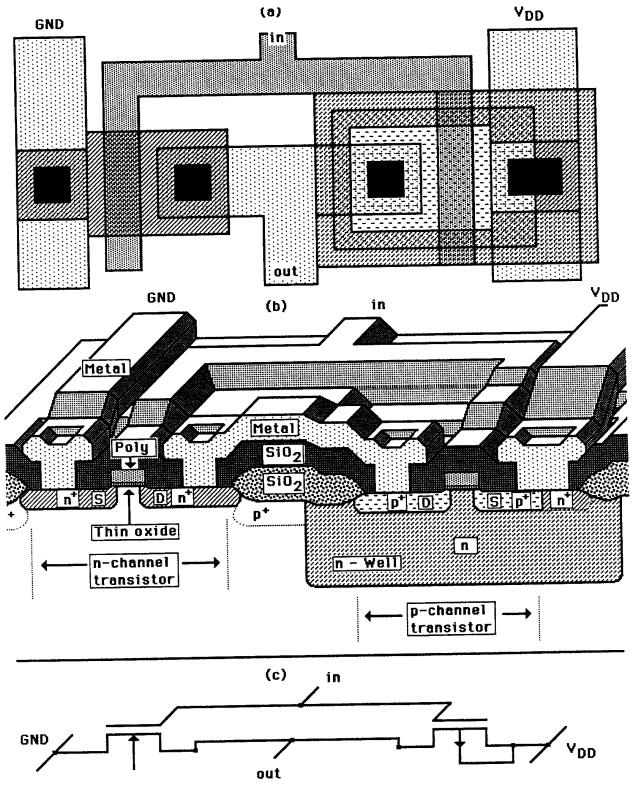

Figure 5-12: CMOS inverter. Composite layout (a), cross-section (b), and electrical diagram (c).

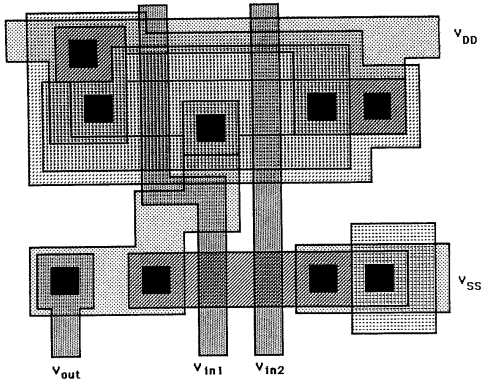

Figure 5-14: Composite layout of the CMOS NAND gate

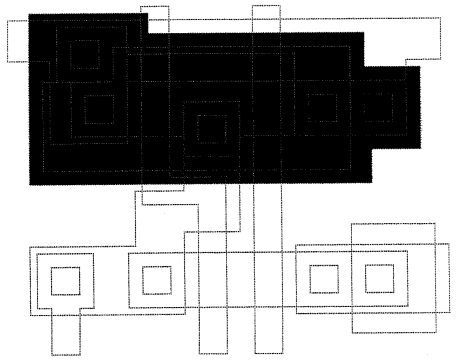

Figure 5-15: Well implant in the n-well CMOS NAND gate.

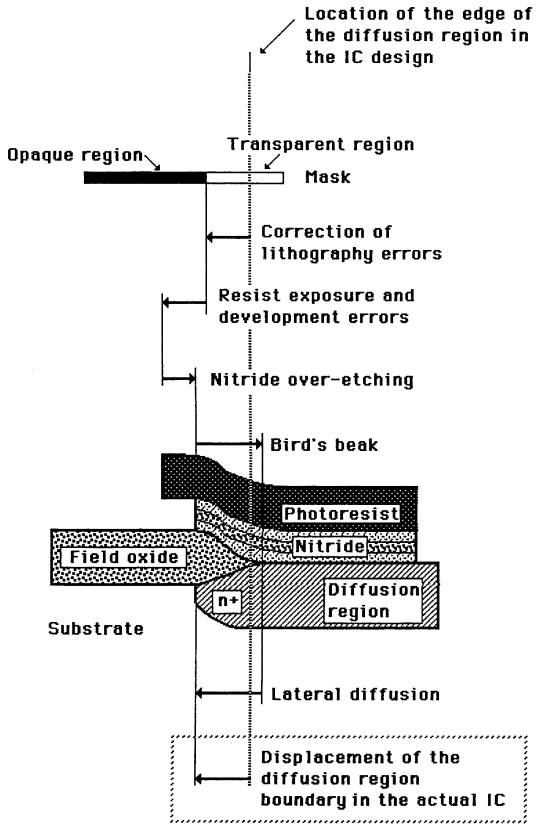

Figure 2-5: Line registration errors in the location of the diffusion region boundary.