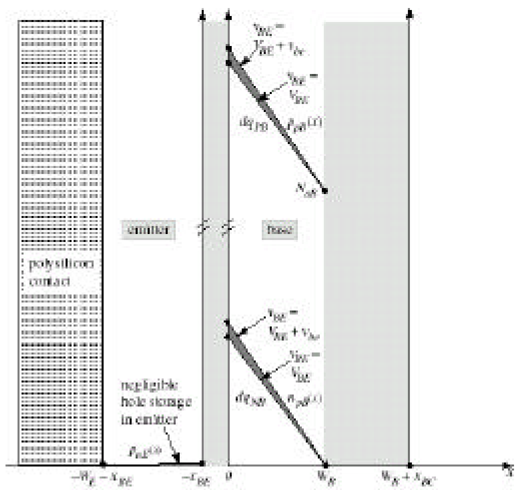
Charge-Storage Elements: Base-Charging Capacitance C_b

- Minority electrons are stored in the base -- this charge q_{NB} is a function of the base-emitter voltage



- base is still neutral... majority carriers neutralize the injected electrons $q_{PB} = q_{NB}$

$$C_b = \left.\frac{\partial q_{PB}}{\partial v_{BE}}\right|_Q$$

Base Transit Time

- The electron charge in the base is found by integrating the electron concentration in the base -- the area is A_E (under the emitter):

$$q_{PB} = -q_{NB} = -\int_0^{W_B} -qA_E n_{pB}(x)dx = \frac{1}{2} qA_E W_B n_{pBo} e^{v_{BE}/V_{th}}$$

- The stored charge is proportional to the collector current:

$$q_{PB} = \frac{1}{2} W_B (W_B/D_{nB}) \left(\frac{qA_E D_{nB}}{W_B}\right) n_{pBo} e^{v_{BE}/V_{th}} = \left(\frac{W_B^2}{2D_{nB}}\right) i_C$$

- The proportionality constant looks like a diffusion time (it is) and is defined as the base transit time:

$$\tau_F = \frac{W_B^2}{2D_{nB}}$$

A typical transit time is τ_F = 10 ps for an oxide-isolated npn BJT.

- The base-charging capacitance is:

$$\boxed{C_b = \left.\frac{\partial q_{PB}}{\partial v_{BE}}\right|_Q = g_m \tau_F}$$

Complete Small-Signal Model

- Add the depletion capacitance from the base-emitter junction to find the total base-emitter capacitance: $C_\pi = C_{jE} + C_b$

$$C_{jE} = \sqrt{2}C_{jEo}$$

C_{jEo} is proportional to the emitter-base junction area (A_E)

- Depletion capacitance from the base-collector junction: C_μ

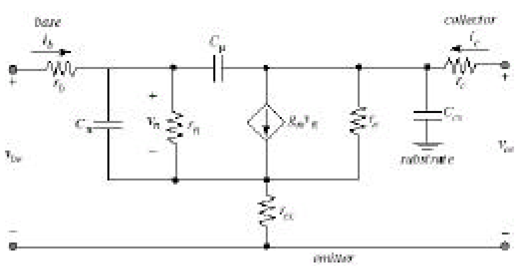
$$C_\mu = \frac{C_{\mu o}}{\sqrt{1 + V_{CB}/\phi_{Bc}}}$$

$C_{\mu o}$ is proportional to the base-collector junction area (A_C)

- Depletion capacitance from collector (n^+ buried layer) to bulk: C_{cs}

$$C_{cs} = \frac{C_{cso}}{\sqrt{1 + V_{CS}/\phi_{Bs}}}$$

C_{cso} is proportional to the collector-substrate junction area (A_S)



npn BJT SPICE model

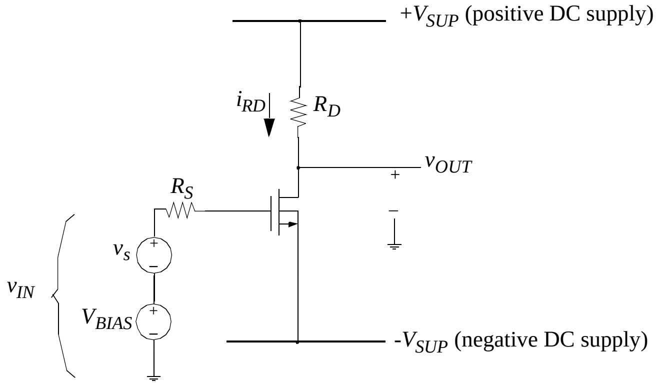
Close correspondence to Ebers-Moll and small-signal models

Name	Parameter Description	Units
IS	transport saturation current [I_S]	Amps
BF	ideal maximum forward beta [β_F]	None
VAF	forward Early voltage [V_{An}]	Volts
BR	ideal maximum reverse beta [β_R]	None
RB	zero bias base resistance [r_b]	Ohms
RE	emitter resistance [r_{ex}]	Ohms
RC	collector resistance [r_c]	Ohms
CJE	B-E zero-bias depletion capacitance [C_{jEo}]	Farads
VJE	B-E built-in potential [ϕ_{Be}]	Volts
MJE	B-E junction exponential factor	None
CJC	B-C zero-bias depletion capacitance [$C_{\mu o}$]	Farads
VJC	B-C built-in potential [ϕ_{Bc}]	Volts
MJC	B-C junction exponential factor	None
CJS	substrate zero-bias depletion capacitance [C_{cso}]	Farads
VJS	substrate built-in potential [ϕ_{Bs}]	Volts
MJS	substrate junction exponential factor	None
TF	ideal forward transit time [τ_F]	Seconds

```
.MODEL MODQN NPN IS=1E-17 BF=100 VAF=25 TF=50P
+ CJE=8E-15 VJE=0.95 MJE=0.5 CJC=22E-15 VJC=0.79 MJC=0.5
+ CJS=41E-15 VJS=0.71 MJS=0.5 RB=250 RC=200 RE=5
```

A Simple MOSFET Amplifier

Amplify = “make something larger” ... something = current, voltage, or power



V_{BIAS} is selected so that V_{OUT} is centered between $+V_{SUP}$ and $-V_{SUP}$:

$$V_{OUT} = 0 \text{ V ... NOT } v_{OUT} = 0 \text{ V!}$$

Find the DC drain current:

$I_{RD} = (V_{SUP} - V_{OUT}) / R_D = V_{SUP} / R_D$

$I_{RD} = I_D = I_{DSAT}$ ... verify that MOSFET is saturated after finding V_{BIAS}

(to find V_{BIAS}, solve saturation current equation for V_{GS} ... the result is that for normal device dimensions and DC drain currents, $V_{GS} = V_{Tn} + (0.25 \text{ to } 0.5)$ V)

MOSFET Amplifier

Now consider the effect of the small signal voltage:

$$v_{IN} = V_{BIAS} + v_s \text{ so } v_{GS} = V_{BIAS} - (-V_{SUP}) + v_s = V_{GS} + v_s$$

Let $v_s(t) = \hat{v}_s \cos(\omega t)$

Approach 1. Just use v_{IN} in the equation for the total drain current and find v_{OUT}

$$v_{OUT} = V_{SUP} - R_D i_D \cong V_{SUP} - R_D(\mu_n C_{ox})\left(\frac{W}{2L}\right)(V_{GS} + v_s - V_{Tn})^2$$

$$v_{OUT} = V_{SUP} - \underbrace{R_D(\mu_n C_{ox})\left(\frac{W}{2L}\right)(V_{GS} - V_{Tn})^2}_{I_D}\left(1 + \frac{v_s}{(V_{GS} - V_{Tn})}\right)^2$$

$$v_{OUT} = V_{SUP} - \underbrace{R_D I_D}_{V_{SUP}}\left(1 + \frac{v_s}{(V_{GS} - V_{Tn})}\right)^2$$

Expand $(1 + x)^2 = 1 + 2x + x^2$

$$\left(1 + \frac{v_s}{V_{GS} - V_{Tn}}\right)^2 = 1 + \frac{2v_s}{V_{GS} - V_{Tn}} + \left(\frac{v_s}{V_{GS} - V_{Tn}}\right)^2$$

Special Case: v_s is "Small"

What's small?

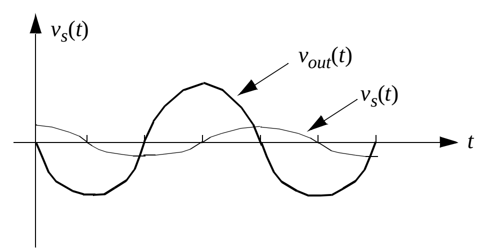
$$\frac{2v_s}{V_{GS}-V_{Tn}} \gg \left(\frac{v_s}{V_{GS}-V_{Tn}}\right)^2 \quad \text{... true if } \frac{2v_s}{V_{GS}-V_{Tn}} \ll 1$$

For this case, the total output voltage is

$$v_{OUT} \cong V_{SUP} - R_D I_D\left(1 + \frac{2v_s}{(V_{GS}-V_{Tn})}\right) = \cancel{V_{SUP}} - \cancel{V_{SUP}} - \frac{2R_D I_D v_s}{(V_{GS}-V_{Tn})}$$

The average output voltage $V_{OUT} = 0$ V so the total output voltage is the small-signal voltage in this special case:

$$v_{OUT} = v_{out} = -\left[\frac{2R_D I_D}{(V_{GS}-V_{Tn})}\right]v_s = -\left[\frac{2V_{SUP}}{(V_{GS}-V_{Tn})}\right]v_s = A_v v_s$$



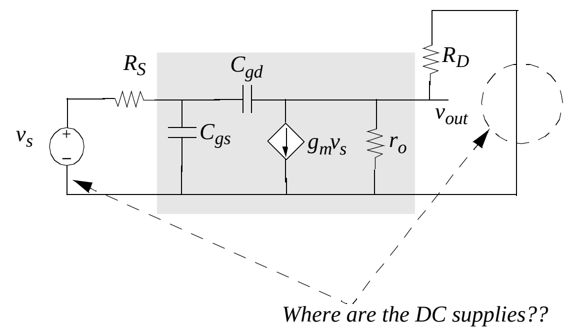
Is There a Better Way?

Approach 2.

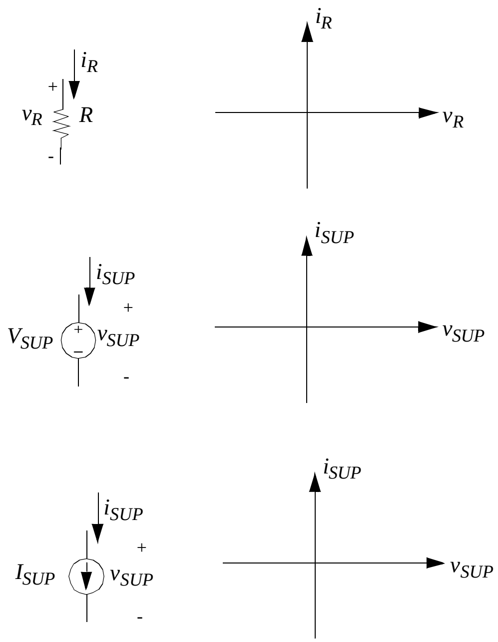
Do problem in two steps.

1. DC voltages and currents (ignore small signals sources): set bias point of of the MOSFET ... we had to do this to pick V_{BIAS} already

2. Substitute the small-signal model of the MOSFET and the small-signal models of the other circuit elements



Small-Signal Models of Two-Terminal Circuit Elements



Small-Signal Model

Small-Signal Output Voltage

Don't bother with capacitors ... wait until Chapter 10 to put them in

$$v_{out} = -g_m v_s (R_D || r_o)$$

Small-signal voltage gain:

$$A_v = -g_m (R_D || r_o)$$

Transconductance of MOSFET in saturation

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{BIAS} - V_{Tn}) = \frac{2I_{DSAT}}{V_{BIAS} - V_{Tn}}$$

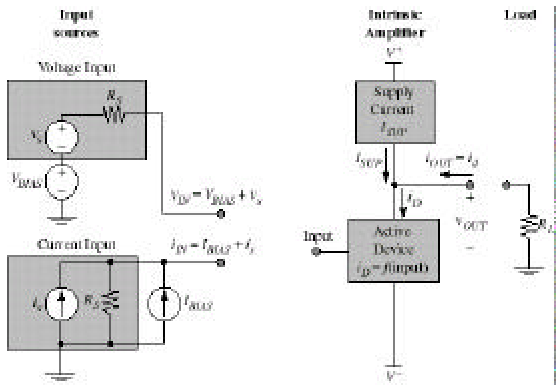
Small-signal voltage gain:

$$A_v = -\left(\frac{2I_{DSAT}}{V_{BIAS} - V_{Tn}}\right)(R_D || r_o)$$

... almost identical to "brute-force result," but the small-signal model includes the effect of channel-length modulation (through $r_o = (1 / \lambda_n I_{DSAT})$)

Generalized Transistor Amplifier

- Perspective: look at the various configurations of bipolar and MOS transistors, for which a *small-signal* voltage or current is transformed (e.g., usually *amplified* -- increased in magnitude) between the input and output ports.
- Amplifier terminology:



Abstractions:

Sources include precisely adjusted bias voltages or currents

Source resistance is associated with the small-signal source

Load resistance typically models another amplifier, speaker, actuator, etc.

Amplifier Biasing

- Input bias voltage V_{IN} sets the DC device current, I_D to precisely equal the supply current I_{SUP}

  (note -- D = "*device*" here)

- Likewise, if the input is the sum of small-signal and DC current sources, then the input bias current I_{BIAS} is chosen so that it sets $I_D = I_{SUP}$

  The DC output current is $I_{OUT} = I_D - I_{SUP} = 0$ A, which implies that the DC output voltage $V_{OUT} = 0$ V also.

Note: both positive and negative DC supply voltages are used so $V_{OUT} = 0$ V does *not* mean that the DC voltage drop is zero!

KEY IDEA: the small-signal voltage or current source perturbs the amplifier bias, through $i_D = f$ (input), which results in a small-signal output current

$i_{OUT} = i_D - i_{SUP} = (I_D + i_d) - I_{SUP} = i_d$

since the supply current is DC ($i_{SUP} = I_{SUP}$)

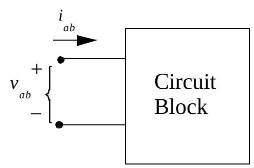
A small-signal output voltage is generated

$v_{out} = - R_L\, i_{out}$, where R_L is the load resistor

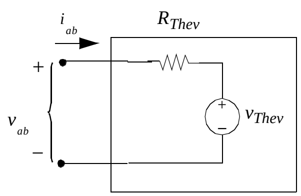
Source and Load Models are "One-Ports"

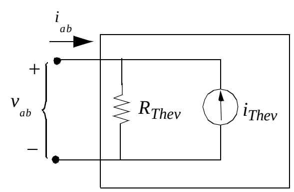
- What is a "port"?

a terminal pair across which a voltage and associated current are defined



- If the circuit block contains only linear elements, then it can be represented as (according to Thevenin's and Norton's Theorems)

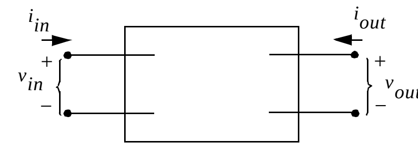




We have "one-port" models for the source and load ...

what about for the amplifier block?

Small-Signal *Two-Port* Models for Amplifier Blocks



Linear and Unilateral: If $v_{in} = 0$, $i_{in} = 0$ and $i_{in} \propto v_{in}$

$$\frac{v_{in}}{i_{in}} \equiv R_{in}$$

But, output depends linearly on what's connected both at input and output: (αs are constants)

$$\left.\begin{array}{lll} \text{e.g.,} & i_{out} = \alpha_1 v_{in} + \alpha_2 v_{out} & (1) \\ \text{or} & i_{out} = \alpha_3 i_{in} + \alpha_4 v_{out} & (2) \\ \text{or} & v_{out} = \alpha_5 v_{in} + \alpha_6 i_{out} & (3) \\ \text{or} & v_{out} = \alpha_7 i_{in} + \alpha_8 i_{out} & (4) \end{array}\right\} \begin{array}{c}\text{ALL EQUIVALENT} \\ \text{(only need one)}\end{array}$$

Two-Port Amplifier Models

- How do we characterize an amplifier's response to a general input signal (Thévenin or Norton source)?

  the controlled source is determined by output signal
  (voltage or current ... we select which is of interest) and by the input signal

  Therefore, there are **FOUR** types of amplifiers:

  Voltage

  Current

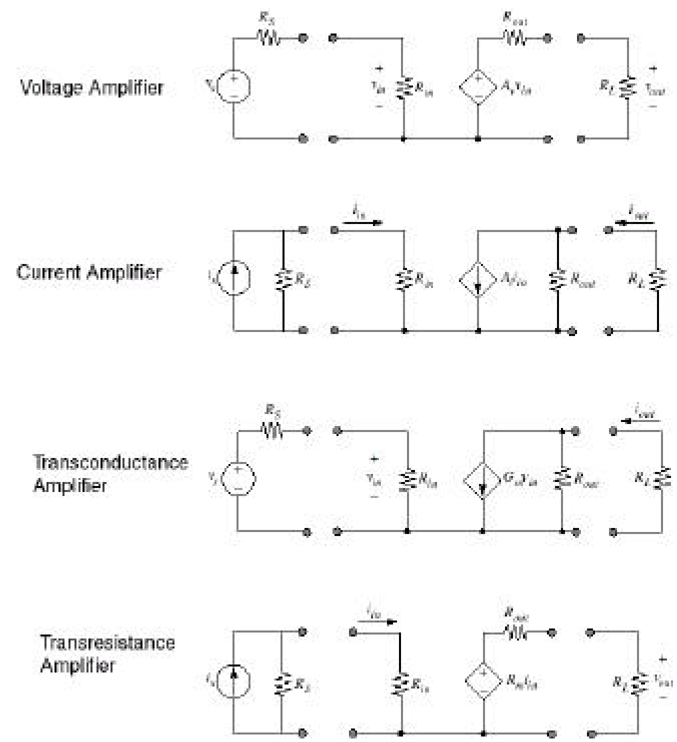
  Transconductance (voltage in, current out)

  Transresistance (current in, voltage out)

- We need *methods* to find the parameters for these four models for a particular transistor amplifier configuration:

R_{in} = Input Resistance	R_{out} = Output Resistance
A_v = Voltage Gain	A_i = Current Gain
G_m = Tranconductance	R_m = Transresistance

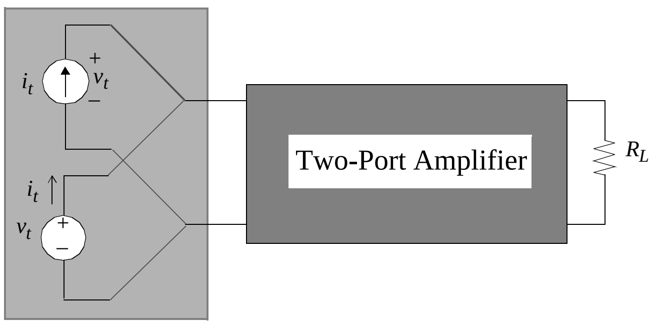
Two-Port Small-Signal Amplifiers



Input Resistance R_{in}

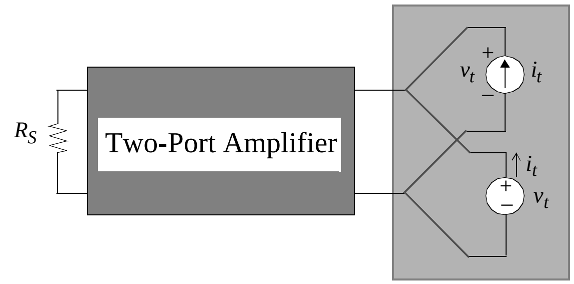
- Define systematic procedures to find the two-port parameters
- **Key idea**: leave the *load* resistance R_L attached when finding R_{in}
- Apply a small-signal *test source* (voltage source **or** current source) and compute (using KVL, KCL, or inspection) the resulting current or voltage:

$$\boxed{R_{in} = \frac{v_t}{i_t}}$$



Output Resistance R_{out}

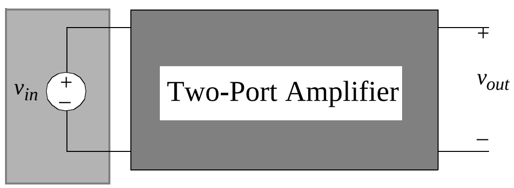
- Remove R_L; leave the source resistance attached when finding R_{out}



$$\boxed{R_{out} = \frac{v_t}{i_t}}$$

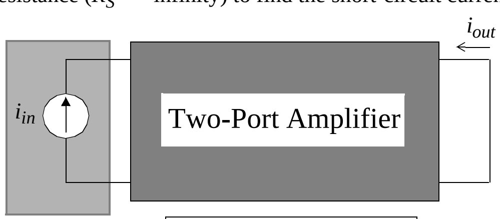
Voltage Gain A_v and Current Gain A_i

- **Voltage gain**: open-circuit the output port (R_L --> infinity) and short the source resistance (R_S --> 0 Ω) to find the unloaded voltage gain A_v:



$$A_v = \left.\frac{v_{out}}{v_{in}}\right|_{R_S = 0,\ R_L \to \infty}$$

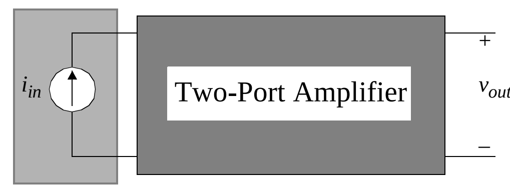
- Current gain: short-circuit the output port (R_L --> 0 Ω) and open-circuit the source resistance (R_S --> infinity) to find the short-circuit current gain A_i:



$$A_v = \left.\frac{i_{out}}{i_{in}}\right|_{R_S \to \infty,\ R_L = 0}$$

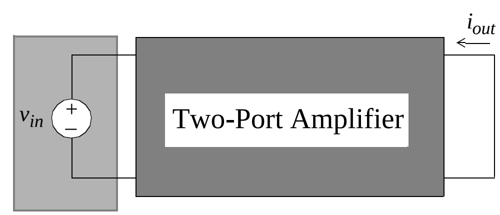
Transresistance R_m and Transconductance G_m

- Open-circuit the source resistance (R_S --> infinity)and open-circuit the output port (R_L --> infinity) to find the transresistance R_m:



$$R_m = \left.\frac{v_{out}}{i_{in}}\right|_{R_S \to \infty,\ R_L \to \infty}$$

- Short-circuit the input resistance (R_S = 0 Ω) and short-circuit the output port (R_L = 0 Ω) to find the transconductance G_m:



$$G_m = \left.\frac{i_{out}}{v_{in}}\right|_{R_S = 0,\ R_L = 0}$$

- Note that the source resistor R_S and the load resistor R_L are *disconnected* for determining the bias point