1. Design the following circuit for a small-signal voltage gain $v_0/v_i$ of 40. Use bias currents $I_{D1} = 100\mu A$ and $I_{C2} = 100\mu A$. Pick the values for $V_{bias}$, $R_D$, $R_C$, $R_E$, and $W/L$ of $M1$. Make sure that $M1$ is in saturation and $Q2$ is in forward active. Note that there is more than one possible solution to this problem. Use the following transistor parameters:

MOS:
- $\mu_nC_{ox} = 50 \mu A/V^2$
- $\lambda_n = 0.05 \text{ V}^{-1}$
- $V_{th} = 0.7 \text{ V}$

BJT:
- $V_A = 30 \text{ V}$
- $\beta = 100$
- $V_{CE,sat} = 0.2 \text{ V}$

$V_{dd} = 5 \text{ V}$. 
2. In this problem, you will analyze the bipolar current source shown below. Assume that \( I_{S1} = I_{S2} \).

\[ V_{dd} = 5 \, \text{V}. \]

![Bipolar Current Source Diagram]

a. For the ideal case, if \( \beta = \infty, V_A = \infty \), what is large signal \( I_{out}/I_{in} \)?

b. Now let \( \beta = 100, V_A = \infty \). Find the new value of \( I_{out}/I_{in} \). Do not make the approximation that \( 1/\beta \ll 1 \).

c. Now \( \beta = \infty, V_A = 20 \, \text{V} \). Find \( I_{out}/I_{in} \).

3. In the circuit below, \( V_{dd} = 5 \, \text{V} \), \( I_{bias} = 100 \, \mu\text{A} \), \( (W/L)_{M2} = 10\mu\text{m}/1\mu\text{m} \). Find \( (W/L)_{M1}, (W/L)_{M3} \), and \( V_{bias} \) for a small signal voltage gain \( v_o/v_i \) of 50 and an output resistance of \( 10 \, \text{k}\Omega \). Make sure all transistors are in saturation for your choice of values. MOS data are as in problem 1, with \( V_{Tn} = V_{Tp}, \lambda_n = \lambda_p, \) and \( \mu_n C_{ox} = \mu_p C_{ox} \).

Why is biasing the circuit this way a bad idea? (Hint: think of what would happen if \( V_{bias} \) was slightly off from what you wanted it to be.)

![CMOS Circuit Diagram]