Lecture 11

• Last time:
  – pn junctions: thermal equilibrium
  – pn junctions: charge-voltage characteristic

• Today:
  – pn junction *small-signal* capacitance
    (attention: this concept is difficult)

Junction Capacitance $C_j$

• Slope of charge-voltage plot is the ratio of the small-signal charge to the small-signal voltage

$$slope = \left. \frac{dq_j}{dv_D} \right|_{v_D} = \frac{q_j}{v_d}$$

• Define the slope (units: $C/V = F$) to be the *junction capacitance* $C_j$
Junction Capacitance vs. DC Bias

Small-Signal Circuit Model

- total voltage and total charge:

\[ v_D \]

\[ V_D < 0 \text{ V} \]

- small-signal variables only →

\[ q_j = Q_J + q_J \]

\[ v_d \]

\[ C_j(V_D) \]

\[ q_j \]

\[ -q_j \]
MOS Structure

Thermal Equilibrium
Charged bi-layer forms: + charges on gate, - in substrate
Built-in voltage between gate and substrate
Applying a DC Voltage $V_{GB}$

**Goal:** find out how the gate charge $Q_G$ varies as a function of the applied voltage $V_{GB}$

**Procedure:**

- start at thermal equilibrium
  
  (i) go negative until built-in charge is cancelled
  
  (ii) keep going until charge on gate is negative
  
  (iii) go positive from thermal equilibrium
  
  (iv) keep increasing $V_{GB}$ until ...

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**IMPORTANT:** IDENTIFY CHARGE IN SUBSTRATE

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Cancel the Built-in Voltage

Apply $V_{FB}$ to “zero” the built-in voltage

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The diagram shows a semiconductor device with labels for $V_{GB}$, $V_{FB}$, and charge density $\rho(x)$.
### Accumulation

\[ V_{GB} < V_{FB} \]

The accumulation region is formed when the gate voltage is less than the flat band voltage. The interface charge is given by:

\[ Q_G \]

### Depletion: \( V_{GB} > V_{FB} \)

\[ V_{FB} < V_{GB} < V_{TH} \]

The depletion region is formed when the gate voltage is greater than the flat band voltage. The interface charge is given by:

\[ Q_G \]

\[ \rho(x) \]

\[ X_d \]