Lecture 18

• Last time:
  – pn junctions under *forward* bias ($V_D = 0.7$ V)

• Today:
  – DC and small-signal model of the forward-biased diode

pn Junctions in ICs
Large-Signal Model

Small-Signal Model: \( r_d \)

Forward-bias assumed \( \rightarrow V_D = 0.7 \) V (approx)

\[
i_D(t) = I_O \left( e^{v_D(t)/V_{th}} - 1 \right) = I_O e^{v_D(t)/V_{th}}
\]

Substitute \( v_D(t) = V_D + v_d(t) \):
Power Series Expansion

\[ e^x = 1 + x + \frac{1}{2} x^2 + \frac{1}{3!} x^3 + \ldots \]

Can quantify the limit of the linear approximation

Graphical Interpretation
Diffusion Capacitance

Depletion region narrows under forward bias, increasing capacitance to $C_j = 1.4 \ C_{jo}$

Dominant capacitance is from storage of minority carriers in the diode’s p and n regions: the *diffusion* capacitance

![Diffusion Capacitance Diagram](image)

Physics of Diffusion Capacitance
Diffusion Capacitance

Minority carrier charge storage is proportional to the DC diode current:

\[ C_d = \left( \frac{I_D}{V_{th}} \right) \tau_T = g_d \tau_T \]

where \( \tau_T \) is the diode’s transit time