Design a MOS amplifier capable of driving a 100Ω load from a 1kΩ source with a voltage gain of 15 and a 3 dB frequency of 1 GHz. Use a 3V supply voltage and minimize the circuit power consumption. Verify your design with SPICE AC and TRAN analysis. You may use any number of transistors in your design and one ideal DC current source. If desired, you may AC couple the load and provide a DC bias voltage via the source. The minimum channel length is $0.25\mu m$. The minimum sized junction (source or drain) is $1\mu m$. Include the source and drain areas in your SPICE netlist instance parameterization as follows:

```
Mx nd ng ns nbody W=w L=l AS=w*1u AD=w*1u PD=w+2u PS=w+2u
```

All NMOS transistors have a ground body contact whereas the PMOS body is tied to either source or VDD.

Use the following transistor models (Warning: These values are different from last homework):

```
model modp pmos level=1 kp=260u vto=-.4 tox=4n lambda=.1 gamma=.55 phi=.87
cj=1e-4 mj=.6 pb=.85 cgso=.2n cgdo=.2n
```

```
model modn nmos level=1 kp=500u vto=.4 tox=4n lambda=.1 gamma=.6 phi=.7
cj=1e-4 mj=.6 pb=.85 cgso=.2n cgdo=.2n
```