Overview

- Last lecture
  - Frequency Response of the Common Source Amplifier

- This lecture
  - Common Gate / Common Drain (Section 10.5, 10.6)
  - Multi-Stage Amplifiers
Recap: Open Circuit Time Constants

- This is a technique to find the dominant pole of a circuit (only valid if there really is a dominant pole!)
- For each capacitor in the circuit you calculate an equivalent resistor “seen” by capacitor and form the time constant $\tau_i = R_i C_i$
- The dominant pole then is the sum of these time constants in the circuit

$$\omega_{p,\text{dom}} = \frac{1}{\tau_1 + \tau_2 + \cdots}$$

Method of Open Circuit Time Constants

Method of open circuits time constants

$$A(j\omega) = A_0 \frac{N(j\omega)}{1 + a_1 j\omega + a_2 (j\omega)^2}$$

- Finding $a_1$:
  - For each capacitor in the circuit you calculate an equivalent resistor “seen” by capacitor and form the time constant $\tau_i = R_i C_i$
  - Equivalent resistor $R_i$ of capacitor $C_i$ found by open circuiting all other capacitors (and eliminating all independent sources) and determining the Thevenin-like resistance as seen from $C_i$. Repeat for all capacitors.

$$a_1 = \sum \tau_i$$

- For dominant pole: $\omega_1 = 1/a_1$
Gain-Bandwidth Product

Result from Miller:

\[ \omega_{p1}^{-1} \approx (R_S) \left( C_{gs} + (1 + g_m R'_{out}) C_{gd} \right) \]

Low-frequency gain:

\[ A_{vo} = \left. \frac{v_{out}}{v_s} \right|_{R_S, R_L} = -g_m R'_{out} \]

Gain-Bandwidth Product

Considering only the first pole (assuming zero and 2\textsuperscript{nd} pole are at much higher frequencies):

\[ |A_v(j\omega)|_{\text{dB}} \]

\[ |A_v(j\omega)| \approx \left| \frac{A_{vo}}{1 + j\omega/\omega_{p1}} \right| \approx \frac{A_{vo}}{\omega/\omega_{p1}} = \frac{A_{vo}\omega_{p1}}{\omega} \]

\[ |A_v(j\omega_u)| = 1 \rightarrow \omega_u = A_{vo}\omega_{p1} \]
Gain-Bandwidth Product

For common-source amplifier:

\[
|A_{vo}|_{\omega p1} = \frac{g_m R'_{out}}{R_S C_{gs} + R_S (1 + g_m R'_{out}) C_{gd}}
\]

Special case: \( R_S \approx R_L < r_o, r_{oc} \)

\[
|A_{vo}|_{\omega p1} \approx \frac{g_m R_L}{R_S (C_{gs} + g_m R_L C_{gd})} \ll \omega_T \quad \text{not that great!}
\]

Common-Drain Amplifier

\[
I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2
\]

\[
V_{GS} = V_T + \frac{2I_{DS}}{\mu C_{ox} \frac{W}{L}}
\]

Weak \( I_{DS} \) dependence
Two-Port CD Model with Capacitors

Ignore $g_{mb}$

Find Miller capacitor for $C_{gs}$ -- note that the gate-source capacitor is between the input and output

Voltage Gain $A_{vCgs}$ Across $C_{gs}$

$$A_{vC_{gs}} = \frac{R_L}{R_L + R_{out}} \approx 1$$

This gain is independent of $C_{gs}$

$$C_{in} = C_{gd} + C_M = C_{gd} + (1 - A_{vCgs})C_{gs}$$

$$C_{in} = C_{gd} + \frac{1}{1 + g_m R_L} C_{gs}$$

$$C_{in} \approx C_{gd}$$
Bandwidth of CD Amplifier

Input low-pass filter’s –3 dB frequency:

$$\omega_p^{-1} = R_S \left( \frac{C_{gd} + \frac{C_{gs}}{1 + g_m R_L}}{1 + g_m R_L} \right)$$

Substitute favorable values of $R_S$, $R_L$:

$R_S \approx 1/g_m \quad R_L >> 1/g_m$

$$\omega_p^{-1} \approx \left( \frac{1}{g_m} \right) \left( C_{gd} + \frac{C_{gd}}{1 + B/G} \right) \approx C_{gd} / g_m$$

Model not valid at these high frequencies

$$\omega_p \approx g_m / C_{gd} > \omega_T$$

Bandwidth of the Common-Gate Amplifier
Two-Port CG Model with Capacitors

No Miller-transformed capacitor!
Unity-gain frequency is on the order of $\omega_T$ for small $R_L$

Summary of Single-Stage Amplifiers

- **CS**: suffers from Miller-magnified capacitor for high-gain case
- **CD**: Miller transformation $\rightarrow$ nulled capacitor $\rightarrow$ “wideband stage”
- **CG**: no Miller capacitor $\rightarrow$ wideband stage (for low load resistance)
Multistage Amplifiers

Necessary to meet typical specifications for any of the 4 types

We have 2 flavors (NMOS, PMOS) of CS, CG, and CD

What are the constraints?

1. Input/output resistance matching

2. DC coupling (no passive elements to block the signal)
   … why not?

Start: Two-Stage Voltage Amplifier

• Use two-port models to explore whether the combination “works”

\[ R_{in} = R_{in1} \rightarrow \infty \]
\[ R_{out} = R_{out2} \rightarrow R_L // r_0 \]

Results: \[ R_{in} = R_{in1}, R_{out} = R_{out2}, A_v = A_{v1} \times A_{v2} \]
Bandwidth of a Cascaded Stages

- Assume identical stages, same dominant pole, $\omega_p$

$$A_{TOT}(j\omega) = \left(\frac{A_0}{1 + j\omega/\omega_p}\right)^N$$

$$|A_{TOT}| = \left|\frac{A_0}{\sqrt{1 + (\omega/\omega_p)^2}}\right|^N$$

$$\frac{1}{\sqrt{2}} A_0^N = \left(\frac{A_0}{\sqrt{1 + (\omega_{BW}/\omega_p)^2}}\right)^N$$

$$\frac{\omega_{BW}}{\omega_p} = \sqrt{2^{1/N} - 1}$$

- $N = 2; \omega_{BW} = 0.64\omega_p$
- $N = 3; \omega_{BW} = 0.51\omega_p$

Adding a Common Drain driver

- $CS_1$
- $CS_2$
- $CD_3$

Input resistance: $\infty$

Voltage gain (2-port parameter): $(g_m r_0)^2 \times 1$

Output resistance: $\sim 1/g_m$
Multistage Current Buffers

Are two cascaded common-gate stages better than one?

\[ CG_1 \quad CG_2 \]

Input resistance: \( R_{in} = R_{in1} \)

Voltage gain: \( A_{v1} \cdot \frac{R_{in2}}{R_{in2} + R_{out1}} \cdot A_{v2} = g_m r_0 \cdot \frac{1}{\frac{1}{g_m} + r_0} \cdot g_m r_0 \approx g_m r_0 \)

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Common-Gate 2\(^{nd}\) Stage

\[ R_{out} = R_{out2} \approx r_{02} \left( 1 + g_{m2} R_{S2} \right) || r_{oc2} \]
Summary of Cascaded Amplifiers

General goals:

1. Boost the gain parameter (except for buffers)
2. Optimize the input and output resistances

\[
\begin{array}{c|c|c}
\text{Voltage:} & R_{in} & R_{out} \\
\text{Current:} & Hi & Lo \\
\text{Transconductance:} & Hi & Hi \\
\text{Transresistance:} & Lo & Lo \\
\end{array}
\]

Second Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available

Output of one stage is directly connected to the input of the next stage \(\rightarrow\) must consider DC levels … why?
Alternate CS-CS Cascade

Use a PMOS CS Stage:

![Circuit Diagram]

Complete Amplifier

![Circuit Diagram]
Another Example: CD-CD cascade

Each CD stage requires $V_{GS} = V_{T0} + V_{d, sat}$
→ Leads to high DC bias required at input of 1st stage

Alternative CD-CD Cascade

Solution: Use a PMOS CD Stage
→ DC level shifts upward
CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case: \( I_{\text{BIAS2}} = 0 \, \text{A} \)

CG Cascade: Sharing a Supply

First stage has no current supply of its own → its output resistance is modified