Why multi-stage?

- Improve gain
- Improve input / output resistance to match environment
Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination “works”

\[ R_{in} = R_{in1} \rightarrow \infty \quad R_{out} = R_{out2} \rightarrow R_L//r_o \]

Results:

\[ R_{in} = R_{in1}, \quad R_{out} = R_{out2}, \quad A_v = A_{v1} \cdot A_{v2} \]
**Voltage Amplifier**

- Should have low output resistance to effectively drive \( RL \)
- Add Common-Drain (Source Follower) Stage

\[ \begin{align*} 
CS_1 & \quad CS_2 & \quad CD_3 
\end{align*} \]

Input resistance: \( \infty \)

Voltage gain (2-port parameter): \( (g_m * r_0)^2 \times 1 \)

Output resistance: \( \sim 1/g_m \)

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**Transconductance Amplifier**

- Should have high input and output resistance and high \( G_m \)

\[ \begin{align*} 
CS_1 & \quad CS_2 & \quad CG_3 
\end{align*} \]

Add common gate stage

Input resistance: \( \infty \)

Transconductance: \( A_1 g_{m2} \)

Output resistance: \( r_d // r_{oc} \)
Adding Common Gate Stage

Input resistance: $\infty$

Voltage gain (2-port parameter): $A_1g_{m2}.r_{out2}/(r_{out2}+1/gm_3)$

Output resistance: $r_{oc}\parallel\left(g_{m2}R_s\right)$ with $R_s = r_{out2}$

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Summary of Cascaded Amplifiers

**General goals:**

1. Boost the gain parameter (except for buffers)
2. Optimize the input and output resistances

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$R_{in}$</th>
<th>$R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage:</td>
<td>Hi</td>
<td>Lo</td>
</tr>
<tr>
<td>Current:</td>
<td>Lo</td>
<td>Hi</td>
</tr>
<tr>
<td>Transconductance:</td>
<td>Hi</td>
<td>Hi</td>
</tr>
<tr>
<td>Transresistance:</td>
<td>Lo</td>
<td>Lo</td>
</tr>
</tbody>
</table>
Second Design Issue: DC Coupling

_Constraint:_ large inductors and capacitors are not available

Output of one stage is directly connected to the input of the next stage → must consider DC levels … why?

Alternate CS-CS Cascade

Use a PMOS CS Stage:
Multistage Current Buffers

Are two cascaded common-gate stages better than one?

\[ R_{in} = R_{in1} \]

Voltage gain:

\[ A_{v1} \cdot \frac{R_{in2}}{R_{in2} + R_{out1}} \cdot A_{v2} = g_m r_0 \cdot \frac{1/g_m}{1/g_m + r_0} \cdot g_m r_0 \approx g_m r_0 \]

CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case:
\[ I_{BIAS2} = 0 \text{ A} \]
CG Cascade: Sharing a Supply

First stage has no current supply of its own → its output resistance is modified

The Cascode Configuration

Common source / common gate cascade is one version of a cascode (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own
Cascode Two-Port Model

Output resistance of first stage = \( R_{\text{out,CS}} = r_{o1} \)

\[
R_{\text{out}} = r_{oc2} \parallel (1 + g_m r_{o1}) r_{o2}
\]

\( G_m = g_{m1} \)

\( R_{in} = \infty \)

Why is the cascode such an important configuration?

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Miller Capacitance of Input Stage

Find the Miller capacitance for \( C_{gd1} \)

Input resistance to common-gate second stage is low → gain across \( C_{gd} \) is small.
Two-Port Model with Capacitors

Miller capacitance:

\[ C_M = (1 - A_{V_{C_{gd1}}}) C_{gd1} \]

\[ A_{V_{C_{gd1}}} = -g_{m1} \left( \frac{1}{g_{m2} || r_{o1}} \right) \approx - \frac{g_{m1}}{g_{m2}} = -1 \]

\[ C_M = 2C_{gd1} \]

Other contributions
Improved Current Sources

Goal: increase $r_{oc}$
Approach: look at amplifier (?) output resistance results … to see topologies that boost resistance

Cascode (or Stacked) Current Source

Insight: $V_{GS2} = \text{constant}$ AND $V_{DS2} = \text{constant}$

Small-Signal Resistance $r_{oc}$:
Drawback of Cascode I-Source

Minimum output voltage for all transistors saturated:

\[ V_{OUT,MIN} = V_{DS4,SAT} + V_{S4} = V_{DS4,SAT} + V_{GS2} \]

Complete Amplifier Schematic
Complete Amplifier Schematic

Goals: $g_{m1} = 1 \text{ mS}, R_{out} = 10 \ \text{M}\Omega$

Device Sizes

$M_1$: select $(W/L)_1 = 200/2$ to meet specified $g_{m1} = 1 \text{ mS}$

$\rightarrow$ find $V_{BIAS} = 1.2 \text{ V}$

Cascode current supply devices: select $V_{SG} = 1.5 \text{ V}$

$(W/L)_4 = (W/L)_3B = (W/L)_3 = (W/L)_3B = 64/2$

$M_2$: select $(W/L)_2 = 50/2$ to meet specified $R_{out} = 10 \ \text{M}\Omega$

$\rightarrow$ find $V_{GS2} = 1.4 \text{ V}$

Match $M_2$ with diode-connected device $M_{2B}$.

Assuming perfect matching and zero input voltage, what is $V_{OUT}$?
**Output (Voltage) Swing**

Maximum $V_{OUT}$

Minimum $V_{OUT}$

**Two-Port Model**

Find output resistance $R_{out}$

$\lambda_n = (1/20) \text{ V}^{-1}$, $\lambda_p = (1/50) \text{ V}^{-1}$ at $L = 2 \mu m \rightarrow$

$r_{on} = (100 \mu A / 20 \text{ V}^{-1})^{-1} = 200 \text{ k}\Omega$, $r_{op} = 500 \text{ k}\Omega$

$g_{m2} = \frac{2I_{D2}}{V_{GS2} - V_{Tn}} = \frac{2(100\mu A)}{1.4V - 1V} = 500\mu S$

$g_{m3} = \frac{2(-I_{D3})}{V_{SG3} + V_{Tp}} = \frac{2(100\mu A)}{1.5V - 1V} = 400\mu S$

$R_{out} = r_{oc} \parallel r_{o2}(1 + g_{m2}R_{S2}) = r_{o3}(1 + g_{m3}R_{S3}) \parallel r_{o2}(1 + g_{m2}r_{o1})$