EE105 - Fall 2006
Microelectronic Devices and Circuits

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Lecture 6: MOSCAP
Overview

- **Announcements**
  - Labs start this week
  - Lab report guide posted on website
  - HW2 and HW1 solutions posted

- **Last lecture**
  - Diode operation

- **This lecture**
  - Diode wrap-up (fabrication and small signal model)
  - MOS capacitor
Diode IV relation is an exponential function

This exponential is due to the Boltzmann distribution of carriers versus energy

For reverse bias the current saturations to the drift current due to minority carriers
Fabrication of IC Diodes

- Start with p-type substrate
- Create n-well to house diode
- p and n+ diffusion regions are the cathode and anode
- N-well must be reverse biased from substrate
- Parasitic resistance due to well resistance
Diode Small Signal Model

- The I-V relation of a diode can be linearized
Diode Small Signal Model

- Expand the current equation to find s-s resistance:

\[
I_D + i_D = I_S \left( e^{\frac{q(V_d + v_d)}{kT}} - 1 \right) \approx I_S e^{\frac{qV_d}{kT}} e^{\frac{qv_d}{kT}}
\]

\[
e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots
\]

\[
I_D + i_D \approx I_D \left( 1 + \frac{q(V_d + v_d)}{kT} + \cdots \right)
\]

\[
i_D \approx \frac{qv_d}{kT} = g_d v_d
\]
Diode Capacitance

- We have already seen that a reverse biased diode acts like a capacitor since the depletion region grows and shrinks in response to the applied field. The capacitance in forward bias is given by

\[ C_j = A \frac{\varepsilon_S}{X_{dep}} \approx 1.4C_{j0} \]

- But another charge storage mechanism comes into play in forward bias
- Minority carriers injected into p and n regions “stay” in each region for a while
- On average additional charge is stored in diode
Charge Storage

- Increasing forward bias increases minority charge density
- By charge neutrality, the source voltage must supply equal and opposite charge
- A detailed analysis yields:

\[ C_d = \frac{1}{2} \frac{qI_d}{kT} \tau \]

Time to cross junction (or minority carrier lifetime)
Diode Circuits

- Rectifier (AC to DC conversion)
- Peak detector (AM demodulator)
- DC restorer
- Clamp
- Voltage doubler / quadrupler /...
MOS Capacitor

- MOS = Metal Oxide Silicon
- Sandwich of conductors separated by an insulator
- “Metal” is more commonly a heavily doped polysilicon layer
- n⁺ or p⁺ layer
- NMOS → p-type substrate, PMOS → n-type substrate

\[
\varepsilon_{ox} = 3.9 \varepsilon_0 \quad \text{Very Thin!} \quad t_{ox} \sim 1 \text{nm}
\]

\[
\varepsilon_s = 11.7 \varepsilon_0
\]
Under thermal equilibrium, the n-type poly gate is at a higher potential than the p-type substrate

\[ \phi_p = -\frac{kT}{q} \ln \frac{N_a}{n_i} \]

\[ \phi_{n^+} \approx 550 \text{mV} \]

No current can flow because of the insulator but this potential difference is accompanied with an electric field

Fields terminate on charge!
At equilibrium there is an electric field from the gate to the body. The charges on the gate are positive. The negative charges in the body come from a depletion region.
If we apply a bias, we can compensate for this built-in potential

\[ V_{FB} = -(\phi_{n^+} - \phi_p) \]

In this case the charge on the gate goes to zero and the depletion region disappears.

In solid-state physics lingo, the energy bands are “flat” under this condition.
Accumulation

If we further decrease the potential beyond the “flat-band” condition, we essentially have a parallel plate capacitor.

- Plenty of holes and electrons are available to charge up the plates.
- Negative bias attracts holes under gate.

\[ Q_G = C_{ox} (V_{GB} - V_{FB}) \]

\[ Q_B = |Q_G| \]

Body (p-type substrate)
Depletion

- Similar to equilibrium, the potential in the gate is higher than the body
- Body charge is made up of the depletion region ions
- Potential drop across the body and depletion region

\[ V_{GB} > V_{FB} \]

\[ Q_G (V_{GB}) = -Q_B \]

\[ Q_B = -qN_a X_d (V_{GB}) \]
As we further increase the gate voltage, eventually the surface potential increases to a point where the electron density at the surface equals the background ion density

\[ n_s = n_i e^{q\phi_s/kT} = N_a \quad \rightarrow \quad \phi_s = -\phi_p \]

At this point, the depletion region stops growing and the extra charge is provided by the inversion charge at surface
Threshold Voltage

- The threshold voltage is defined as the gate-body voltage that causes the surface to change from p-type to n-type.
- For this condition, the surface potential has to equal the negative of the p-type potential.
- We’ll derive that this voltage is equal to:

\[ V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\varepsilon_s N_a (-2\phi_p)} \]
Inversion Stops Depletion

- A simple approximation is to assume that once inversion happens, the depletion region stops growing.
- This is a good assumption since the inversion charge is an exponential function of the surface potential.
- Under this condition:

\[ Q_G(V_{Tn}) \approx -Q_{B,\text{max}} \]

\[ Q_G(V_{GB}) = C_{ox} (V_{GB} - V_{Tn}) - Q_{B,\text{max}} \]
In accumulation, the charge is simply proportional to the applies gate-body bias.

In inversion, the same is true.

In depletion, the charge grows slower since the voltage is applied over a depletion region.
Numerical Example

- **MOS Capacitor with p-type substrate:**
  \[ t_{ox} = 20\text{nm} \quad N_a = 5 \times 10^{16} \text{cm}^{-3} \]

- **Calculate flat-band:**
  \[ V_{FB} = - (\phi_{n^+} - \phi_p) = -(550 - (-402)) = -0.95\text{V} \]

- **Calculate threshold voltage:**
  \[
  V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\varepsilon_s N_a (-2\phi_p)}
  \]
  \[
  V_{Tn} = -0.95 - 2(-0.4) + \frac{\sqrt{2 \times 1.6 \times 10^{-19} \times 1.04 \times 10^{-12} \times 5 \times 10^{16} \times 2 \times 0.4}}{C_{ox}} = 0.52\text{V}
  \]
Num Example: Electric Field in Oxide

- Apply a gate-to-body voltage:
  \[ V_{GB} = -2.5 < V_{FB} \]

- Device is in accumulation

- The entire voltage drop is across the oxide:
  \[ E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{V_{GB} + \phi_n - \phi_p}{t_{ox}} = \frac{-2.5 + 0.55 - (-0.4)}{2 \times 10^{-6}} = -8 \times 10^5 \frac{V}{cm} \]

- The charge in the substrate (body) consist of holes:
  \[ Q_B = -C_{ox} (V_{GB} - V_{FB}) = 2.67 \times 10^{-7} \text{ C/cm}^2 \]
Numerical Example: Depletion Region

- In inversion, what’s the depletion region width and charge?

\[ V_{B,\text{max}} = \phi_s - \phi_p = -\phi_p - \phi_p = -2\phi_p = 0.8\,\text{V} \]

\[ V_{B,\text{max}} = \frac{1}{2} \left( \frac{qN_a}{\varepsilon_s} \right) X_{d,\text{max}}^2 \]

\[ X_{d,\text{max}} = \sqrt{\frac{2\varepsilon_s V_{B,\text{max}}}{qN_a}} = 144\,\text{nm} \]

\[ Q_{B,\text{max}} = -qN_a X_{d,\text{max}} = -1.15 \times 10^{-7}\,\text{C/cm}^2 \]
MOS CV Curve

- Small-signal capacitance is slope of Q-V curve
- Capacitance is linear in accumulation and inversion
- Capacitance in depletion region is smallest
- Capacitance is non-linear in depletion
In accumulation mode the capacitance is just due to the voltage drop across $t_{ox}$.

In inversion the incremental charge comes from the inversion layer (depletion region stops growing).

In depletion region, the voltage drop is across the oxide and the depletion region.

\[ C_{dep} = \frac{\varepsilon_s}{x_{dep}} \]

\[ C_{tot} = \frac{C_{dep}C_{ox}}{C_{dep} + C_{ox}} = \frac{C_{ox}}{1 + C_{dep}C_{ox}} = \frac{C_{ox}}{1 + \frac{\varepsilon_s}{\varepsilon_{ox}} \frac{t_{ox}}{x_{dep}}} \]