EE105 – Fall 2014
Microelectronic Devices and Circuits

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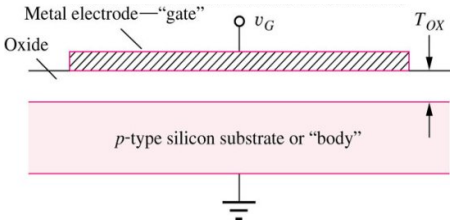
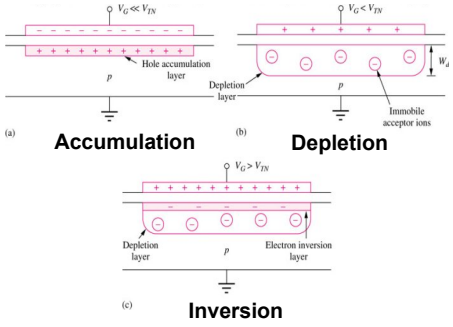
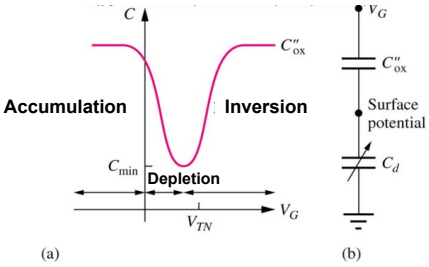
MOS (Metal-Oxide-Semiconductor) Capacitor Structure



- **First electrode - Gate: Consists of low-resistivity material such as metal or doped polycrystalline silicon**
- **Second electrode - Substrate or Body: *n*- or *p*-type semiconductor**
- **Dielectric - Silicon dioxide: stable high-quality electrical insulator between gate and substrate.**

MOS Capacitors in Three Bias Regions



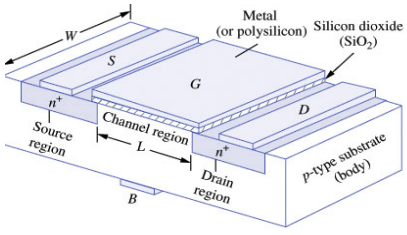


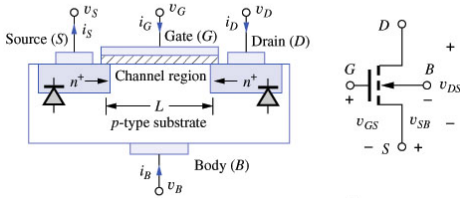
Threshold voltage: V_{TN}
Gate voltage: V_G

- **Accumulation: $V_G << V_{TN}$**
- **Depletion: $V_G < V_{TN}$**
- **Inversion: $V_G > V_{TN}$**

- **Total capacitance modeled as series combination of fixed oxide capacitance and voltage-dependent depletion-layer capacitance.**

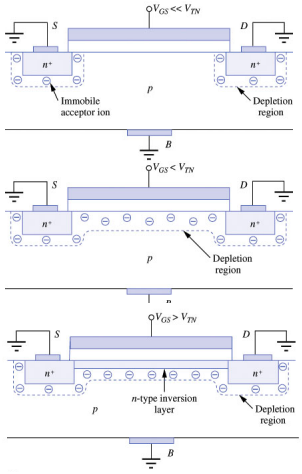
NMOS Transistor Structure





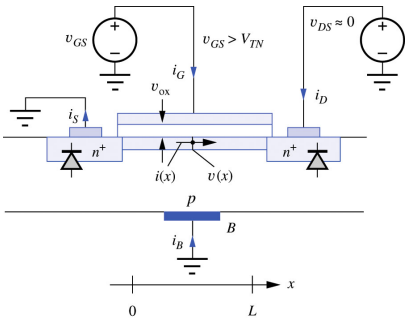
- **4 device terminals: Gate(G), Drain(D), Source(S) and Body(B).**
- **Source and drain regions form pn junctions with substrate.**
- **v_{SB}, v_{DS} and v_{GS} always positive during normal operation.**
- **v_{SB} always < v_{DS} and v_{GS} to reverse bias pn junctions**

NMOS Transistor: Qualitative I-V Behavior



- $V_{GS} << V_{TN}$: Only small leakage current flows.
- $V_{GS} < V_{TN}$: Depletion region formed under gate merges with source and drain depletion regions. No current flows between source and drain.
- $V_{GS} > V_{TN}$: Channel formed between source and drain. If $v_{DS} > 0$, finite i_D flows from drain to source.
- $i_B = 0$ and $i_G = 0$.

NMOS Transistor: Triode Region Characteristics



$$K_n = \mu_n C_{ox}^{"} \left(\frac{W}{L}\right)$$

$C_{ox}^{"} = \varepsilon_{ox}/T_{ox}$: oxide capacitance per unit area

ε_{ox} = oxide permittivity (F/cm)

T_{ox} = oxide thickness (cm)

Charge per unit length in channel:

$$Q'(x) = -WC_{ox}^{"}(v_{GS} - v(x) - V_{TN}) \qquad \text{[F/cm]}$$

$v(x)$: voltage of channel at position x

$$i(x) = Q'(x)v_x(x),$$

$v_x(x)$: electron velocity at x

$$v_x(x) = -\mu_n E_x = -\mu_n \frac{dv(x)}{dx}$$

μ_n : electron mobility

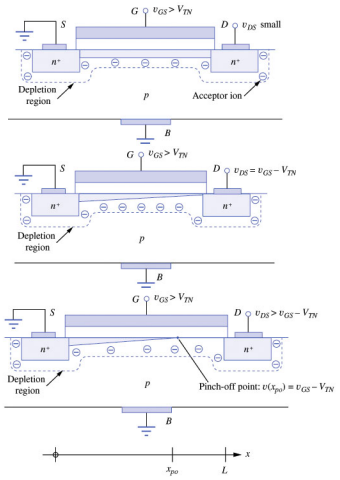
$$\int_0^L i(x)\,dx = \int_0^L W\mu_n C_{ox}^{"}(v_{GS} - v(x) - V_{TN})\frac{dv(x)}{dx}dx$$

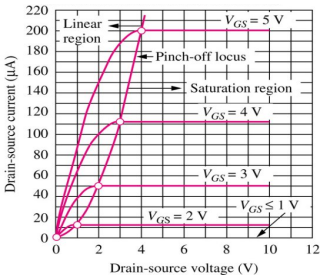
$$i_D L = \int_0^{v_{DS}} W\mu_n C_{ox}^{"}(v_{GS} - v(x) - V_{TN})dv(x)$$

$$i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}$$

for $v_{GS} - V_{TN} \geq v_{DS} \geq 0$

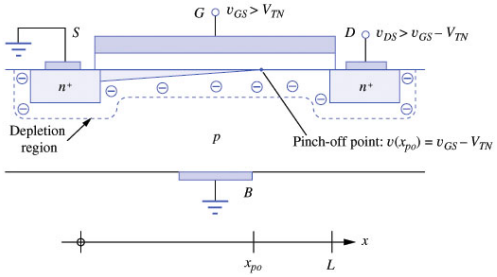
NMOS Transistor: Saturation Region





- If v_{DS} increases above triode region limit, the channel region disappears and is said to be pinched-off.
- Current saturates at constant value, independent of v_{DS}.
- Saturation region operation mostly used for analog amplification.

NMOS Transistor: Saturation Region (cont.)



$$i_D = \frac{\mu_n C_{ox}''}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2 \quad \text{for} \quad v_{DS} \ge v_{GS} - V_{TN}$$

$v_{DSAT} = v_{GS} - V_{TN}$ is termed the saturation or pinch-off voltage

Transconductance of an MOS Device

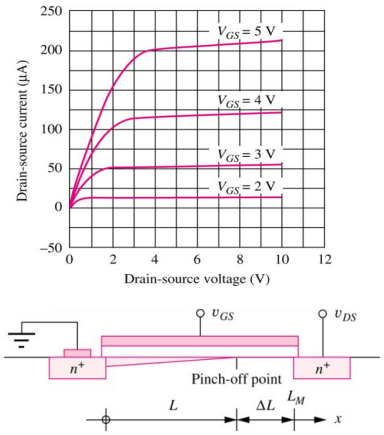
- **Transconductance relates the change in drain current to a change in gate-source voltage**

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q-pt}$$

- **Taking the derivative of the expression for the drain current in saturation region,**

$$g_m = \mu_n C_{ox}^{"} \frac{W}{L}\left(V_{GS} - V_{TN}\right) = \frac{2I_D}{V_{GS} - V_{TN}}$$

Channel-Length Modulation

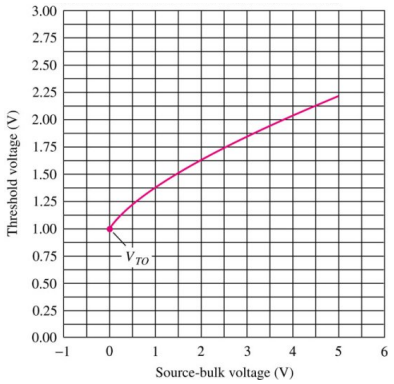


- **As v_{DS} increases above v_{DSAT}, the length of the depleted channel beyond the pinch-off point, DL, increases and the actual L decreases.**
- **i_D increases slightly with v_{DS} instead of being constant.**

$$i_D = \frac{\mu_n C_{ox}^{"}}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2\left(1 + \lambda v_{DS}\right)$$

λ = channel length modulation parameter

Body Effect or Substrate Sensitivity



- **Non-zero v_{SB} changes threshold voltage, causing substrate sensitivity modeled by**

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

where

V_{TO} = threshold voltage for $v_{SB} = 0$

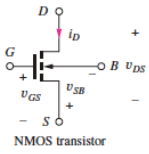
γ = body - effect parameter $\left(\sqrt{\text{V}}\right)$

$2\phi_F$ = surface potential (V)

NMOS Model Summary

NMOS TRANSISTOR MATHEMATICAL MODEL SUMMARY

Equations (4.24) through (4.28) represent the complete model for the i-v behavior of the NMOS transistor.



For all regions,

$$K_n = K_n' \frac{W}{L} \qquad K_n' = \mu_n C_{ox}'' \qquad i_G = 0 \qquad i_B = 0 \tag{4.24}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } v_{GS} \le V_{TN} \tag{4.25}$$

Triode region:

$$i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS} \qquad \text{for } v_{GS} - V_{TN} \ge v_{DS} \ge 0 \tag{4.26}$$

Saturation region:

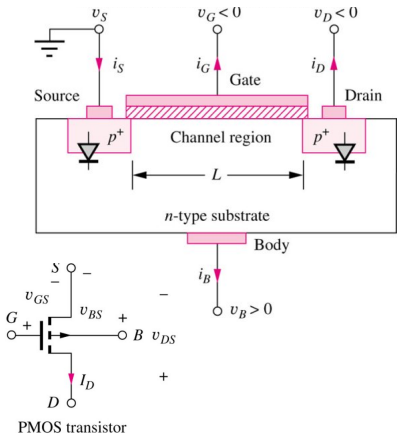
$$i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS}) \qquad \text{for } v_{DS} \ge (v_{GS} - V_{TN}) \ge 0 \tag{4.27}$$

Threshold voltage:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{4.28}$$

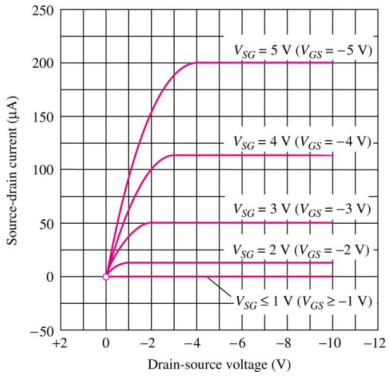
$V_{TN} > 0$ for enhancement-mode NMOS transistors. Depletion-mode NMOS devices can also be fabricated, and $V_{TN} \le 0$ for these transistors.

PMOS Transistors: Enhancement-Mode Structure



- ***p*-type source and drain regions in an *n*-type substrate.**
- **$v_{GS} < 0$ required to create p-type inversion layer in channel region**
- **For current flow, $v_{GS} < V_{TP}$**
- **To maintain reverse bias on source-substrate and drain -substrate junctions, $v_{SB} < 0$ and $v_{DB} < 0$**
- **Positive bulk-source potential causes V_{TP} to become more negative**

PMOS Transistors: Output Characteristics



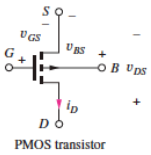
- **For $v_{GS} > V_{TP}$, transistor is off.**
- **For more negative v_{GS}, drain current increases in magnitude.**
- **PMOS device is in the triode region for small values of V_{DS} and in saturation for larger values.**
- **Remember $V_{TP} < 0$ for an enhancement mode transistor**

PMOS Model Summary

PMOS TRANSISTOR MATHEMATICAL MODEL SUMMARY

Equations (4.29) through (4.33) represent the complete model for the i-v behavior of the PMOS transistor.

For all regions,



PMOS transistor

$$K_p = K'_p \frac{W}{L} \qquad K'_p = \mu_p C''_{ox} \qquad i_G = 0 \qquad i_B = 0 \tag{4.29}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } V_{GS} \geq V_{TP} \tag{4.30}$$

Triode region:

$$i_D = K_p\left(v_{GS} - V_{TP} - \frac{v_{DS}}{2}\right)v_{DS} \qquad \text{for } 0 \leq |v_{DS}| \leq |v_{GS} - V_{TP}| \tag{4.31}$$

Saturation region:

$$i_D = \frac{K_p}{2}(v_{GS} - V_{TP})^2(1 + \lambda|v_{DS}|) \qquad \text{for } |v_{DS}| \geq |v_{GS} - V_{TP}| \geq 0 \tag{4.32}$$

Threshold voltage:

$$V_{TP} = V_{TO} - \gamma\left(\sqrt{v_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{4.33}$$

For the enhancement-mode PMOS transistor, $V_{TP} < 0$. Depletion-mode PMOS devices can also be fabricated; $V_{TP} \geq 0$ for these devices.