Closed Book. You may use a calculator. The equation sheets are located on the last two pages of this exam. You may rip those out for your use. Keep the rest of the exam stapled together. You do not need to turn in the equation sheets when turning in the exam.

Problem 1 (15 points):

Problem 2 (30 points):

Problem 3 (25 points):

Problem 4 (30 points):

Total (100 points):
1. (15 points) For each circuit below, draw the output waveform. Assume Op-Amp is ideal, $V_{in} = \sin(\omega t)$, and $R_2 = 2 \times R_1$. For each section, I/V characteristic of diode is given. Clearly label all points and connect to input waveform with dotted line.

(a) (3 points)
(b) (6 points)

Answer:

Diode I/V Characteristic
(c) (6 points)

Answer:
2. (30 points) In this problem you will design the transistor sizes for the amplifier circuit shown below.

We would like to design the circuit such that \( V_O = \frac{1}{2} V_{DD} \).

The parameters of the devices are:

- \( V_{T(M_1)} = 1V \)
- \( V_{T(M_2)} = -2V \)
- \( \mu_N C_{ox} = k'_N = 1mA/V^2 \)
- \( \mu_P C_{ox} = k'_P = 0.5mA/V^2 \)
- \( \lambda_{M1} = 0 \)
- \( \lambda_{M2} = 0 \)

(a) (4 points) Why is \( \frac{1}{2} V_{DD} \) a good choice for the DC voltage at the output of this amplifier circuit? Explain.

(b) (6 points) What is the region of operation for transistor \( M_1 \) if \( V_O = \frac{1}{2} V_{DD} \)? Show your work.
(c) (6 points) What is the region of operation for transistor $M_2$ if $V_O = \frac{1}{2}V_{DD}$? Show your work.

(d) (6 points) If $V_O = \frac{1}{2}V_{DD}$ and $\frac{W_{M1}}{L_{M1}} = 15$, what is the current in transistor $M_1$?
(e) (8 points) If \( \frac{W_{M1}}{L_{M1}} = 15 \), what is the \( \frac{W}{L} \) ratio for transistor \( M_2 \) that results in \( V_O = \frac{1}{2} V_{DD} \)?
3. (25 points) The following is a cross-section of a MOS Capacitor in a silicon wafer. For this problem, use $\Phi_n = 400\text{mV}, \Phi_{p+} = -550\text{mV}, V_{DD} = 0.8\text{V}, V_{TP} = -0.4\text{V}, t_{ox} = 20\text{nm}$. Pay careful attention to voltage polarity!

(a) (6 points) What bias voltage $V_{GB}$ do you need to apply in order to achieve the flat-band condition (no charge in the capacitor)?

(b) (6 points) You decide to use this capacitor to filter noise on the supply $V_{DD}$ (also known as decoupling). To do this you hook up the gate (G) to $V_{DD}$ and the body (B) to ground. What region of operation is the MOS capacitor in? Justify your answer (a guess without justification will receive no credit).
(c) (6 points) You compare this with the opposite configuration of hooking up the
gate (G) to ground and the body (B) to $V_{DD}$. What region of operation is the
MOS capacitor in now? Justify your answer (a guess without justification will
receive no credit).

(d) (7 points) Which configuration gives the highest capacitance per unit area?
Calculate the capacitance per unit area in this preferred configuration.
4. (30 points) A rectangular piece of intrinsic Si semiconductor of length $L = 1 \mu m$, $W = 10 \mu m$ (into the page) and the thickness $t = 2 \mu m$ is shown below. This structure will be referred to as the “body” of a device you will investigate. The connections “drain” and “source” are on the sides as shown.

(a) (4 points) The p-type body is doped with a concentration of $N_A = 10^{18} \text{cm}^{-3}$, what are the free electron and hole concentrations? Explain.

(b) (6 points) If the semiconductor is doped p-type with a concentration of $N_A = 10^{18} \text{cm}^{-3}$, how much current flows if 1V is applied to the drain and the source is tied to ground?
(c) (6 points) Now suppose that heavily doped n-type gates are added to the structure as shown (doped at $10^{19}\text{cm}^{-3}$). The gate voltages are biased with the same positive voltage. What do you expect to happen? Draw a picture and explain your figure. For this part, assume both the drain and source are grounded. Note that there is no oxide layer anywhere in this structure.
(d) (8 points) For a gate bias of 0.5V, calculate the drain-source current when a small $V_{DS}$ is applied. You may leave your answer as a function of $V_{DS}$. Hint: start by calculating the depletion width in the p-type substrate.

(e) (6 points) Can you explain how this structure acts like a voltage controlled resistor? Does the current increase or decrease with increasing gate bias? Explain how the gate controls the channel.
**Guidelines:** Closed book. You may use a calculator.

Do not unstaple the exam. In order to maximize your score, write clearly and indicate each step of your calculations. We cannot give you partial credit if we do not understand your reasoning. You may use the back sides of the exam paper if you need more space, but if you do please clearly label the number and part. You should also make a note next to the problem that there is more work on the back.

The resistance of a material is related to the physical dimensions and resistivity by

\[ R = \frac{\rho L}{tW} = \frac{\rho}{t} \frac{L}{W} = R_{sq} \frac{L}{W} \]

The capacitance of a parallel plate structure is given by

\[ C = \frac{\epsilon A}{d} \]

The conductivity of a material depends on charge density \((n \text{ and } p)\), mobility \(\mu_{n,p}\), and charge of carriers \(q_e\):

\[ \sigma = q_e (\mu_n n + \mu_p p) \]

Note that mobility is defined through the drift velocity, \(v = \mu E\) where \(E\) is the electric field. An intrinsic semiconductor has a doping concentration of \(n_i = p_i = 1.4 \times 10^{10} \, \text{cm}^{-3}\). A pn junction has a built-in potential given by

\[ \phi_{bi} = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2} \]

and a depletion region width of (for a reverse bias voltage of \(V_{rev}\))

\[ W_{dep} = \sqrt{\frac{2\epsilon_s (\phi_{bi} + |V_{rev}|)}{q} \left( \frac{1}{N_a} + \frac{1}{N_d} \right)} \]

where the permittivity of Si is given by

\[ \epsilon_s = 11.9 \times 8.854 \times 10^{-14} \frac{\text{F}}{\text{cm}} \]

The permittivity of SiO\(_2\) is given by

\[ \epsilon_s = 3.9 \times 8.854 \times 10^{-14} \frac{\text{F}}{\text{cm}} \]

The thermal voltage at room temperature \(T\) is given by

\[ V_t = \frac{kT}{q} \approx 26 \text{mV} \]

where \(q = 1.6 \times 10^{-19} \text{C}\) is the charge of an electron.

The current through a forward-biased diode is given by

\[ I_D = I_0 (\exp \left( \frac{qV}{kT} \right) - 1) \]
MOS Square Law Device Physics (Saturation)

\[ I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

In the triode region, we have

\[ I_{DS} = \mu C_{ox} \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) (1 + \lambda V_{DS}) \]

A 3-terminal transistor can be represented by its small-signal equivalent circuit shown below: