Basic Semiconductor Fabrication

EE143
300mm and 450mm Si Wafers

- Current: **300mm wafers**
- Next gen: **450mm wafers**
- **200mm wafers** are still workhorse, particularly for IoT
- **Economy of scale**
  - Full CMOS has 60+ photomasks, and yet chip cost almost nothing
  - $1K for **200mm**
    - $ $ /mm$^2$ $0.013/mm^2$
  - $10K for **300mm**
    - $ $ /mm$^2$ $0.14/mm^2$

http://wccftech.com/foundries-tsmc-companies-shift-300mm-wafers/
Basic Semiconductor Fabrication Process

Learn more in EE 143

(0)
- P-Si

(1)
- SiO₂
- P-Si
- SiO₂

(2)
- UV
- Mask
- Photo resist
- SiO₂
- P-Si

(3)
- SiO₂
- SiO₂
- P-Si

- Si wafer
- Add material
- Deposition
- Lithography
- Photomask
- Photo-sensitive
- Development
- Remove material
- Etching
State of the Art Lithography Machine
(EUV: Extreme Ultra Violet)

- UV Lamp
- Mask
- Photoresist
- Wafer
- Exposure, Step
- UV Laser $\rightarrow 193 \text{ nm}$
- Immersion Lithography

- H$_2$O $n = 1.3$
- Lens
- Resolution $d \sim \frac{\lambda}{2n}$
- Expensive Camera
- stepper
- soft X-ray $\lambda = 13 \text{ nm}$
State of the Art Lithography Machine
(EUV: Extreme Ultra Violet)
Microfabrication (cont’d)

(4) Arsenic implantation

(5) SiO₂  SiO₂

(6) Al

+ As⁺

10 keV
100 keV
1 MeV
Microfabrication (cont’d)
Microfabrication (cont’d)

(9) Si₃N₄
SiO₂
N⁺
P
Al
(10) Si₃N₄
SiO₂
N⁺
P
Al

Dry etch

Al

Applied Materials
LAM

Wire

Plastic package
Metal leads
Modern CMOS IC Cross Section

Intel 14nm Broadwell chip, side-on, showing all 13 layers

\[ R = \rho \frac{L}{A} \]

Power
Ground

MOS transistor

Cu

Metal interconnect