EE105 – Fall 2015
Microelectronic Devices and Circuits: MOSFET

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Simplest Model of MOSFET (from EE16B)

**N-type MOSFET (NMOS)**
- **Gate**
- **Drain** $V_{\text{gate}} = V_{GS}$
- $V_{DS} > 0$
- $I_{DS} > 0$
- **Source**

**Case 1.** $V_{\text{gate}} < V_{th,N}$  

**ON** State

**Case 2.** $V_{\text{gate}} > V_{th,N}$  

**OFF** State

**P-type MOSFET (PMOS)**
- **Gate**
- **Drain** $V_{\text{gate}} = V_{SG}$
- $V_{SD} > 0$
- $I_{SD} > 0$
- **Source**

**Case 1.** $V_{\text{gate}} < V_{th,P}$  

**OFF** State

**Case 2.** $V_{\text{gate}} > V_{th,P}$  

**ON** State
CMOS Inverter

Why is the PMOS Drain here?

High PMOS

$V_{\text{DD}}$

NMOS

$V_{\text{in}}$

$V_{\text{out}}$

$V_{\text{OUT}}$

High

Low
CMOS NAND Gate

\[ O = \overline{A \cdot B} \]

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More Circuit Symbol for NMOS

(a) 4 terminal including Body (Arrow pointing to channel indicating substrate is p-type)

(b) Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)

(c) Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Note in NMOS
1. Drain voltage is always more positive than Source voltage
2. Current always flows from Drain to Source
More Circuit Symbol of PMOS

4 terminal including Body
(Arrow pointing away from channel indicating substrate is n-type)

Modified circuit symbol with arrow on source
(Arrow indicating direction of current flow)

Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Note in PMOS
1. Source voltage is always more positive than Drain voltage
2. Current always flows from Source to Drain
3. Source is usually drawn on top so current flows downward (convention)
Analog Voltage Amplifier

$V_{DS} = V_D - V_S$

DC bias at Quiescent (Q) point
Small-signal input superimposed on a DC bias voltage
Symbol used in this course: $V_{GS} = V_{GS} + v_{gs}$

Need to know the transistor’s I-V characteristics to find the voltage gain (and other properties of the amplifier)
I-V Curves of NMOS (for fixed Gate Voltage)

Current flows when $v_{GS} > V_{tn}$ (threshold voltage)

More positive gate voltage

Triode

Saturation Region

Increase $V_{GS}$

$V_{GS,1}$

$V_{GS,2}$

$V_{GS,3}$

$V_{GS,4}$

$V_{DS}$

$V_{DS}$

$V_{DS}$

$V_{DS}$

$V_{DS}$
Drain Current vs Gate Voltage

\[ i_D = \frac{1}{2} k_n (v_{GS} - V_{tn})^2 = \frac{k_n}{2} V_{ov}^2 \]

“Square Law”

\[ V_{ov} = V_{GS} - V_{tn} \]

“Over Drive”

\[ V_{tn} \]

Threshold

NMOS
MOSFET Device Structure

- **MOSFET**: metal-oxide-semiconductor field effect transistor

- **Typically**
  - Channel length: $L \sim < 10 \text{ nm} \text{ to } 0.35 \mu\text{m}$,
  - Channel width: $W \sim 0.05 \mu\text{m} \text{ to } 100 \mu\text{m}$,
  - Oxide thickness: $t_{ox} \sim 1 \text{ to } 10 \text{ nm}$

\[ \text{Dielectric constant per unit area} \]

- $\text{SiO}_2$: $\varepsilon_r = 3.9$
- $\text{HfO}_2$: $\varepsilon_r \left( \frac{1}{t_{ox}} \right)$
NMOSFET (or simply NMOS)

- **N-channel MOSFET**
  - Current conducted by electrons

- **3 terminal device**
  - Source (S): n+ (heavily n-type)
  - Drain (D): n+
  - Gate (G): metal deposited on insulator above channel

- Substrate (called “Body”) is a 4\textsuperscript{th} terminal
  - Substrate is p-doped

- Electrons is induced in channel when a positive gate voltage is applied

- Electrons moves from Source to Drain
  - Current flows from D to S
Creating a “Channel” for Current Flow

MOS is a capacitor across an insulator (oxide). When a positive voltage is applied at Gate, electrons are induced under the gate. At "threshold", sufficient number of electrons form a "channel" between Source and Drain, forming a conductive channel.

Total charge in the channel:

\[ |Q| = C_{ox} \cdot W \cdot L \cdot (v_{GS} - V_t) = C \cdot \Delta V \]

where \( C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \) is oxide capacitance per unit area.

\( \varepsilon_{ox} = 3.9 \varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} \text{ F/m} \)

\( W \): gate width

\( L \): gate length

\( V_t \): Threshold voltage

\( v_{GS} - V_t \equiv v_{OV} \) is called "Overdrive Voltage"
Large-Signal Model

(usually used to solve DC bias voltage and current)
When $v_{OV} = v_{GS} - V_t > 0$, a channel is formed between Source and Drain.

Linear charge density in channel:

$$\frac{|Q|}{L} = C_{ox} W \cdot v_{OV}$$

Electric field along the channel

$$|E| = \frac{v_{DS}}{L}$$

Drain current = charge density x velocity:

$$i_D = \frac{|Q|}{L} v_n = \frac{|Q|}{L} \mu_n |E| = C_{ox} W \cdot v_{OV} \mu_n \frac{v_{DS}}{L}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS}$$

At small $v_{DS}$, the transistor is like a gate-controlled variable resistor.
Current at Small $v_{DS}$

\[ i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS} \]
\[ \bar{i}_D = \frac{1}{2} k_n \cdot v_{OV}^2 \]

\[ = k_n \frac{W}{L} v_{OV} v_{DS} \]
\[ = k_n v_{OV} v_{DS} \]

where

\[ k_n = \mu_n C_{ox} \cdot \frac{W}{L} \] : process transconductance parameter

\[ k_n = \mu_n C_{ox} \cdot \frac{W}{L} \] : MOSFET transconductance parameter

MOSFET behaves like a linear resistor

\[ r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{k_n v_{OV}} \]

Resistance value can be changed by gate voltage (overdrive voltage)
Triode Region ($v_{DS} < v_{OV}$)

As $v_{DS}$ increases, the potential in the channel is no longer a constant. Assume the channel is $v(x)$:

$$i_D = C_{ox} W (v_{GS} - v(x) - V_t) v_n(x)$$

$$v_n(x) = \mu_n |E(x)| = \mu_n \frac{dv(x)}{dx}$$

Note: $i_D$ is still constant along the channel (think Kirchhoff's Current Law)

Integrate along the channel

$$\int_{x=0}^{x=L} i_D \, dx = \int_{x=0}^{x=L} \left( C_{ox} W (v_{GS} - v(x) - V_t) \mu_n \frac{dv(x)}{dx} \right) \, dx$$

Change of variable on right-hand side: $x \rightarrow v$

$$i_D L = \int_{v=0}^{v=v_{DS}} \left( C_{ox} W (v_{OV} - v) \mu_n \right) \, dv$$

$$i_D = \mu_n C_{ox} \frac{W}{L} \left( v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$
Triode Region ($v_{DS} < v_{OV}$)

When $0 \leq v_{DS} \leq v_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L} \left( v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$

This is called the "Triode Region"

$$v_{DS} = v_{OV} \Rightarrow C_D = (\mu_n C_{ox} \frac{W}{L}) \frac{1}{2} v_{OV}^2 = \frac{1}{2} k_n v_{OV}^2$$

$V_{DS} = V_{OV} = V_{GS} - V_{tn}$

Net charge at Drain

$$= C_{ox} \cdot W \cdot (V_{GS} - V_{DS} - V_{tn})$$

$$= 0$$
Pinch-Off

The channel potential at the drain side is $v_{DS}$. When $v_{DS} = v_{OV}$, the local charge density there

$$\frac{|Q|}{\text{area}} = C_{ox} \left(v_{GS} - v_{DS} - V_t\right) = C_{ox} \left(v_{OV} - v_{DS}\right) = 0$$

So the channel is "pinched off" near the Drain. Once the channel is pinched off, the drain current remains constant:

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2$$

This region, $v_{DS} > v_{OV}$, is called "Saturation"
Saturation Region \((v_{DS} > v_{OV})\)

![Graph showing the saturation region of a transistor with equations and annotations]

When \(0 \leq v_{DS} \leq v_{OV}\)

\[
i_D = \mu_n C_{ox} \frac{W}{L} \left( v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)
\]

This is called the "Triode Region"

When \(v_{DS} > v_{OV}\)

\[
i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2
\]

This is called "Saturation Region"
Full I-V Curves of NMOSFET

$V_{tn}$: threshold voltage of NMOS
In Saturation Region

\[ i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2 \]

\[ = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_m)^2 = \frac{1}{2} k_n V_{OV}^2 \]

To experimentally determine \( V_m \):

Measure and plot \( \sqrt{i_D} \) versus \( v_{GS} \)

\[ \sqrt{i_D} = \sqrt{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_m)} \]

\( V_m = \) intercept with horizontal axis
PMOSFET (or simply PMOS)

- **P-channel MOSFET**
  - Current conducted by holes

- **3 terminal device**
  - Source (S): p+ (heavily p-type)
  - Drain (D): p+
  - Gate (G): metal deposited on insulator above channel

- **Substrate (called “Body”)** is a 4\(^{th}\) terminal
  - Substrate is n-doped

- Holes is induced in channel when a negative gate voltage is applied

- Holes moves from Source to Drain
  - Current flows from S to D
CMOS
(Complementary MOS)

- CMOS is the prevalent IC technology today
- Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a “well”
- PMOS is placed in an “n well” here.
- Alternatively, NMOS can be placed in p well