Prelab report  Extended to next week.
One-Port Models (EECS 16A)

• A terminal pair across which a voltage and associated current are defined

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**Thevenin**

- $v_{ab}$
- $R_{thev}$
- $i_{ab}$

**Norton**

- $v_{ab}$
- $R_{thev}$
- $i_{thev}$
Small-Signal Two-Port Models

• We assume that input port is linear and that the amplifier is \textit{unilateral}:
  \begin{itemize}
  \item Output depends on input
  \item But input is independent of output.
  \end{itemize}

• Output port: depends \textit{linearly} on the current and voltage at the input and output ports

• Unilateral assumption is good as long as “overlap” capacitance is small (MOS)
Two-Port Small-Signal Amplifiers

Voltage Amplifier

Current Amplifier
Two-Port Small-Signal Amplifiers

Transconductance Amplifier

Transresistance Amplifier
Input Impedance $Z_{in}$

- Looks like a Thevenin resistance measurement, but note that the output port has the load resistance attached.

\[
Z_{in} = \left. \frac{v_x}{i_x} \right|_{Z_{S \text{removed}}, Z_{L \text{attached}}}
\]
Output Impedance $Z_{out}$

- Looks like a Thevenin resistance measurement, but note that the input port has the source resistance attached

$$Z_{out} = \frac{v_x}{i_x} \left|_{Z_L \text{ removed}, \ Z_S \text{ attached}} \right.$$
Single-Stage Amplifier Types

- **Common Source (CS)**
  - $A_{v} = -g_{m} R_{o}$
  - $R_{in} = \infty$
  - $R_{out} = R_{o}$
  - $V_{o} = -g_{m} V_{in} - R_{o}$

- **Common Gate (CG)**
  - $A_{v} = -g_{m} R_{o}$
  - $V_{o} = -g_{m} (R_{o} / R_{D})$
  - $R_{o} >> R_{D}$

- **Common Drain (CD)**
  - $A_{v} = g_{m} R_{D}$

Previously:

$A_{i} = \infty$

$A_{i} = -1$
Lab

A few kΩ

\[ v_o = -g_m \cdot R_D \]

\[ \frac{V_{ol}}{R_D} \approx R_0 \]

\[ V_o \text{ think } \sim 200 \text{kΩ} \]

\[ v_{in} \]
Common Gate (CG) Amplifier

DC bias:

\[ I_{SUP} = I_Q = I_{DS} \]

Design \( \Rightarrow V_{GS} \)

Av, \( A_v \), \( \rightarrow \) related to \( g_m \)

\( g_m(I_Q) \rightarrow I_Q \rightarrow V_{GS} \)

select DC Bias Pt

Knows \( g_m \)

\( I_R \)

Input
Common Gate AC Model

\[ V_{DD} \rightarrow \text{Ac Ground} \]

\[ R_D \]

\[ i_{out} \]

\[ R_L \]

\[ R_s \]

\[ i_s \]

Input

Output
Common Gate Small Signal

\[ A_i \]
\[ R_{in} \]
\[ R_{out} \]

\[ v_{gs} \]
\[ g_m v_{gs} \]
\[ i_s \]
\[ i_{out} \]
CG as a Current Amplifier: Find $A_i$

\[ i_{out} = i_d = -i_s \]

\[ \frac{i_{out}}{i_s} = A_i = -1 \]
CG Input Resistance

At input:
\[ i_t = -g_m v_{gs} + \left( \frac{v_t - v_{out}}{r_o} \right) \]

Output voltage:
\[ v_{out} = -i_d \left( R_D \parallel R_L \right) = i_t \left( R_D \parallel R_L \right) \]

\[ i_t = g_m v_t + \left( \frac{v_t - \left( R_D \parallel R_L \right) i_t}{r_o} \right) \]
Approximations...

- We have this messy result:

\[
\frac{1}{R_{in}} = \frac{i_t}{v_t} = \frac{g_m + \frac{1}{r_o}}{1 + \frac{R_D \parallel R_L}{r_o}}
\]

- But we don’t need that much precision. Let’s start approximating:

\[
R_{in} \approx \frac{R_L}{r_o}
\]

\[
R_D \parallel R_L \approx R_L
\]

\[
R_{in} = \frac{1}{g_m}
\]

\[
\frac{R_L}{r_o} \approx 0
\]

\[
R_{in} \sim 2k\Omega
\]

- Large

\[
g_m = 0.5 \text{ mS}
\]

\[
r_o = 200k\Omega
\]

- Small resistance

\[
\text{CG has low } R_{in}
\]
CG Output Resistance

\[ v_{t} = g_{m}v_{gs} + \frac{v_{s} - v_{t}}{r_{o}} = 0 \]

\[ v_{s}\left(\frac{1}{R_{s}} + g_{m} + \frac{1}{r_{o}}\right) = \frac{v_{t}}{r_{o}} \]

\[ v_{gs} = 0 - v_{S} \]
CG Output Resistance

Substituting $v_s = i_t R_S$

$$i_t R_S \left( \frac{1}{R_S} + g_m + \frac{1}{r_o} \right) = \frac{v_t}{r_o}$$

The output resistance is $(v_t / i_t) || R_D$

$$R_{out} = R_D \ || \ \left( R_S \left( \frac{r_o}{R_S} + g_m r_o + 1 \right) \right)$$

$$R_{out} = R_D \ || \ \left( r_o + g_m r_o R_S + R_S \right)$$
Approximating the CG $R_{out}$

The exact result is complicated, so let’s try to make it simpler:

$$g_m \approx 500 \mu S \quad r_o \approx 200k\Omega$$

$$R_{out} \approx R_D \parallel [r_o + g_m r_o R_S + R_S]$$

Assuming the source resistance is less than $r_o$,

$$R_{out} \approx R_D \parallel [r_o + g_m r_o R_S] = R_D \parallel [r_o (1 + g_m R_S)]$$

Current source load, $R_D = \infty$, $R_{out} = R_D + g_m r_o R_S$
CG Two-Port Model

- Function: a *current buffer*
  - Low Input Impedance
  - High Output Impedance
Common Gate as a "V Amplifier"

\[ A_v = \frac{V_{out}}{V_{in}} \]

\[ A_I = -1 \]

\[ -I_{in} = \frac{V_{in}}{g_m} = g_m \cdot V_{in} \]

\[ V_{out} = (-I_{in} \cdot R_{out}) = I_{in} \cdot R_{out} \]

\[ A_v = g_m \cdot R_{out} \]

If we have \( R_b \) load (instead of current source):

\[ R_{out} = R_b // R'_{out} \approx R_b \Rightarrow A_v = g_m \cdot R_b \]
Common-Drain Amplifier

\[ I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2 \]

\[ V_{GS} = V_T + \sqrt{\frac{2 I_{DS}}{\mu C_{ox} \frac{W}{L}}} \]

Weak \( I_{DS} \) dependence
Common Drain AC Schematic
CD Voltage Gain

\[ v_{gs} = v_{in} - v_{out} \]

\[
\frac{v_{out}}{R_L \parallel r_o} = g_m v_{gs}
\]

\[
\frac{v_{out}}{R_L \parallel r_o} = g_m \left( v_{in} - v_{out} \right)
\]
CD Voltage Gain (Cont.)

KCL at source node:

\[
\frac{v_{out}}{R_L \parallel r_o} = g_m \left( v_{in} - v_{out} \right)
\]

\[
\left( \frac{1}{R_L \parallel r_o} + g_m \right) v_{out} = g_m v_{in}
\]

Voltage gain:

\[
\frac{v_{out}}{v_{in}} = \frac{g_m}{1 + \frac{R_L \parallel r_o}{g_m}}
\]

\[
\frac{v_{out}}{v_{in}} \approx \frac{g_m}{1/R_L + g_m} \approx 1
\]
CD Output Resistance

Sum currents at output (source) node:

\[ i_x = g_m v_x \]
\[ R_{out} = r_o \parallel R_L \parallel \frac{v_x}{i_x} \]
\[ R_{out} \approx \frac{1}{g_m} \]
CD Output Resistance (Cont.)

\[ r_o || R_L \ll \frac{1}{g_m} \implies \text{Ignore } r_o || R_L \]

- **Function:** a voltage buffer
  - High Input Impedance
  - Low Output Impedance
Transistor Amplifiers $\rightarrow$ Gm/V/I

Gm Amplifier
Common Source

I-Buffer
Common Gate

V-Buffer
Source Follower