EE105 – Fall 2015
Microelectronic Devices and Circuits
Multi-Stage Amplifiers

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Terminal Gain and I/O Resistances of MOS Amplifiers

<table>
<thead>
<tr>
<th>Common Source (CS)</th>
<th>Common Drain (CD)</th>
<th>Common Gate (CG)</th>
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</thead>
<tbody>
<tr>
<td><img src="image" alt="Common Source Circuit" /></td>
<td><img src="image" alt="Common Drain Circuit" /></td>
<td><img src="image" alt="Common Gate Circuit" /></td>
</tr>
</tbody>
</table>

### Gain and Resistances

**Common Source (CS):**

- \( A_{V,t} = -\frac{g_m R_L}{1 + g_m R_S} \)
- \( R_i = \infty \)
- \( R_o = \left[ r_o (1 + g_m R_S) \right] \)
- \( A_{I,t} = \infty \)

**Common Drain (CD):**

- \( A_{V,t} = \frac{R_L}{1 + \frac{g_m}{R_L}} \)
- \( R_i = \infty \)
- \( R_o = \frac{1}{g_m} \)
- \( A_{I,t} = \infty \)

**Common Gate (CG):**

- \( A_{V,t} = g_m R_L \)
- \( R_i = \frac{1}{g_m} \)
- \( R_o = \left[ r_o (1 + g_m R_E) \right] \)
- \( A_{I,t} \approx 1 \)

### Without Degeneration

- Simply set \( R_S = 0 \)

For the gain, \( R_i \), \( R_o \) of the whole amplifier, you need to include voltage/current dividers at input and output stages.
### Summary of MOS Single-Transistor Amplifiers

<table>
<thead>
<tr>
<th>MOS</th>
<th>Common Source</th>
<th>Common Source with Deg.</th>
<th>Common Drain</th>
<th>Common Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_i$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>Small</td>
</tr>
<tr>
<td>$R_o$</td>
<td>Large</td>
<td>Very Large</td>
<td>Small</td>
<td>Large</td>
</tr>
<tr>
<td>$A_v$</td>
<td>Moderate</td>
<td>Small</td>
<td>$\sim 1$</td>
<td>Moderate</td>
</tr>
<tr>
<td>$f_H$</td>
<td>Small</td>
<td>Moderate</td>
<td>Large</td>
<td>Large</td>
</tr>
</tbody>
</table>
Single Stage Amplifier Cannot Meet All Requirements

• For example, a general purpose operational amplifier requires
  – High input resistance ~ 1MΩ
  – Low output resistance ~ 100Ω
  – High voltage gain ~ 100,000

• No single transistor amplifier can satisfy all spec’s

• Cascading multiple stages of amplifiers offers a path towards the design
Multistage Amplifiers

- Usually
  - An input stage to provide required input resistance
  - Middle stage(s) to provide gain
  - An output stage to provide required output resistance or drive external loads

- More gain!
  - Gain/stage limited, especially in nanoscale devices

- Improve Bandwidth
  - De-couple high impedance nodes from large capacitors

- DC coupling (no passive elements to block the signal)
  - Use amplifiers to naturally “level shift” signal
Impedance “Match”

- On-chip circuits often use “voltage/current” matching to minimize loading
- Keep in mind the input resistance and output resistance of each type of stage so that the loading does not create an undesired effect

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<tr>
<th></th>
<th>Ideal $R_{in}$</th>
<th>Ideal $R_{out}$</th>
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<tbody>
<tr>
<td>Voltage Amplifier</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Current Amplifier</td>
<td>0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transconductance Amplifier</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transresistance Amplifier</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Two-Stage Voltage Amplifier

- Boost gain by cascading Common-Source stages

Can combine into a single 2-port model
Results of new 2-port:  $R_{in} = R_{in1}$, $R_{out} = R_{out2}$
CS Cascade Analysis

Results of new 2-port:

\[ R_{in} = R_{in1} = \infty \]
\[ R_{out} = R_{out2} = R_o || r_{oc} \]
\[ A_V = \frac{V_{out}}{V_{in}} = \frac{V_{int}}{V_{in}}, \quad \frac{V_{out}}{V_{int}} = \left( -g_{m1} \cdot \frac{r_o}{r_{oc}} \right) \cdot \frac{1}{s} \left( -g_{m2} \cdot \left( \frac{r_o}{r_{oc}} \right) \right)^2 \]

\[ = g_{m1} g_{m2} \left( \frac{r_o}{r_{oc}} \right)^2 \]
CS Cascade Bandwidth

Two time constants:

\[ \tau_1 = \frac{(C_{gs} + C_m) - (r_o || r_{oc})}{g_m} \]

\[ \tau_2 = \frac{1}{g_m} \]

\[ C_m = C_{gd}(1-A), \quad A = -g_m(r_o || r_{oc}) \]

\[ C_T = C_{gs} + C_m \]
Bandwidth Extension

- Common Source stage has high gain, but low bandwidth
- Note that Miller effect is the culprit
- Follower stage can buffer source resistance from Miller cap
Bandwidth Extension Using Source Follower (SF)

\[ V_{\text{out}} = \frac{V_{\text{int}}}{V_{\text{in}}} \cdot \frac{V_{\text{in}} + V_{\text{int}}}{V_{\text{in}}} \cdot \frac{V_{\text{out}}}{V_{\text{int}} + V_{\text{int}}} = -g_{m1} \left( r_{o} || r_{oc} \right) \cdot 1 \cdot g_{m2} \left( r_{o} || r_{oc} \right). \]

\[ A_1 = \left( r_{o} || r_{oc} \right) \cdot \left( C_{gs} + C_{m} \right). \]

\[ A_2 = \frac{1}{g_{m}} \left( C_{gs} + C_{gd} \left( 1 + g_{m2} \left( r_{o} || r_{oc} \right) \right) \right) / C_{m}. \]
CS Example with Cap Load

- $C_{in}$ and $C_S$ are very large, therefore they look like short circuits to the AC signal.

- If $C_L$ is very large, its pole dominates, let’s analyze
CS with Cap Load – Small Signal

• What are the time constants associated with the capacitors in this circuit?

• What can we do if we have to drive a large $C_L$?

\[ \tau_1 = (R_1 \parallel R_2)(C_{gs} + C_m) \]
\[ \tau_2 = C_L \left( R_{oL} \parallel R_D \right) \]
How can we reduce the impact of $C_L$?

One way is to reduce the resistance $R_d$, but this reduces our low-frequency gain.

To recover the gain we can increase $g_{m1}$.

What does this cost us?
A better way to extend the bandwidth is to add a source-follower stage.

Similar to previous example.
By adding a CD (Source Follower) we can increase the bandwidth.

It costs us power for the CD stage.

Remember that increasing the BW by increasing $g_{m1}$ costs us much more.

$$T_2 = C_L \cdot \frac{1}{g_{m2}}$$
CS + CG = Cascode

• Common source provides gain, CG acts as a buffer, but is it even helping?

• How do you bias this circuit?
Merged CS + CG = Cascode

- Let’s apply 2-port small-signal analysis

- In this case, we care about the input current to the second stage

- Note that the input resistance of the CG is low, therefore the majority of the CS current is fed to the CG

- \( A_v = \frac{V_{out}}{V_{in}} = \frac{i_{in}}{V_{in}} \cdot \frac{V_{out}}{i_{in}} = g_m \cdot R_{out} \)
Cascode Bandwidth

- Draw in the $C_{gs}$ and $C_{gd}$ capacitors.
- Which ones are Miller effected?
- Is this better or worse than a CS without a CG?

\[ C_m = C_{gd} \left( 1 - (-1)^2 \right) = 2C_{gd} \]
Cascode Bandwidth

- Draw in the capacitors and input resistance

\[ C_M = C_{gd} \left( 1 + \frac{1}{g_m} \right) \]

\[ = C_{gd} \left( 1 + \frac{g_m}{g_{m1}} \right) \approx \frac{2}{2} C_{gd} \]
Cascode Biasing

- CG has a very large output resistance
- Loading it with $R_D$ is likely to reduce the voltage gain
- We can increase the gain by using a current source load, but $r_{oc}$ needs to be very large. Can use a cascode current mirror!
Complete Amplifier Design

Goals: $g_{m1} = 1 \text{ mS}, \ R_{out} = 5 \ \text{M}\Omega$

For simplicity, let’s assume all $g_m$ and $r_o$ values are equal

$A_V \approx -g_{m1}R_{out} = -1 \text{ mS} \times 5 \ \text{M}\Omega = -5,000$

$R_{out} \approx \frac{1}{2} g_m r_o^2 = 5 \ \text{M}\Omega$

$r_o = \sqrt{20 \ \text{M}\Omega} = \sqrt{10 \ \text{M}\Omega} = 100 \ \text{k}\Omega$

$A_V = g_{m1} \cdot r_{out} = g_{m1} \cdot g_{m2} \cdot r_{out} \cdot v^2$
Bias Current & Device Sizing

Need to know process parameters to solve for W/L

\( k' = 100 \ \mu A/V^2 \)
\( \lambda = 0.1 \ [V^{-1}] \)

\[ r_o = \frac{1}{\lambda I_{DS}} = 100k\Omega \]

\[ I_{DS} = \frac{1}{0.1V^{-1} \times 100k\Omega} = 100\mu A \]

\[ g_m = \sqrt{2k'(\frac{W}{L})I_{DS}} = 1mS \]

\[ \frac{W}{L} = \frac{g_m^2}{2k'I_{DS}} = \frac{(1mS)^2}{2 \times 100\mu \times 100\mu A} = 50 \]

\[ V_{in} \]

\[ V_{out} \]

\[ R_G \]
**Output (Voltage) Swing**

Need to know $V_{GS} - V_T$ (e.g. $V_{DSAT}$, $V_{OV}$)

\[
g_m = \frac{2I_{DS}}{V_{GS} - V_T} = 1mS
\]

\[
V_{GS} - V_T = \frac{2I_{DS}}{g_m} = \frac{2 \times 100 \mu A}{1mS} = 0.2V
\]

Maximum $V_{OUT} = \sqrt{0.5}$

Minimum $V_{OUT} = 0.4V$

Input Bias $V_{IN} \leq 0.7V$. 