EE105 – Fall 2015
Microelectronic Devices and Circuits
Multi-Stage Amplifiers

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Terminal Gain and I/O Resistances of MOS Amplifiers

<table>
<thead>
<tr>
<th>Common Source (CS)</th>
<th>Common Drain (CD)</th>
<th>Common Gate (CG)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="a" alt="Common Source Circuit" /></td>
<td><img src="b" alt="Common Drain Circuit" /></td>
<td><img src="c" alt="Common Gate Circuit" /></td>
</tr>
</tbody>
</table>

For the gain, $R_i$, $R_o$ of the whole amplifier, you need to include voltage/current dividers at input and output stages.
For intuition:
Universal treatment of different transistor configuration:

Gain:
\[ \text{CS: } A_v = -g_m R_0 \]
\[ \text{CD: } A_v = 1 \]
\[ \text{CG: } A_v = g_m R_0 \]
\[ A_x = -1 \]

\[ R_G = \infty \]
\[ R_D \approx (g_m R_0) R_{s, \text{ext}} + R_0 \]
In case \( R_{s, \text{ext}} = 0 \)
\[ R_D = R_0 \]
\[ R_S = \frac{1}{g_m} \]

\[ (g_m R_{s, \text{ext}}) R_0 \gg R_0 \gg \frac{1}{g_m} \]
# Summary of MOS Single-Transistor Amplifiers

<table>
<thead>
<tr>
<th>MOS</th>
<th>Common Source</th>
<th>Common Source with Deg.</th>
<th>Common Drain</th>
<th>Common Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_i$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>Small</td>
</tr>
<tr>
<td>$R_o$</td>
<td>Large</td>
<td>Very Large</td>
<td>Small</td>
<td>Large</td>
</tr>
<tr>
<td>$A_V$</td>
<td>Moderate</td>
<td>Small</td>
<td>$\sim 1$</td>
<td>Moderate</td>
</tr>
<tr>
<td>$f_H$</td>
<td>Small</td>
<td>Moderate</td>
<td>Large</td>
<td>Large</td>
</tr>
</tbody>
</table>

- $R_i$ represents the input resistance, and its value is infinite for common source and common source with degeneration configurations.
- $R_o$ is the output resistance and is large for common source and very large for common source with degeneration.
- $A_V$ is the voltage gain, moderate for common source and small for common source with degeneration.
- $f_H$ is the frequency at which the phase shift is $90^\circ$, small for common source and moderate for common source with degeneration.

- Miller capacitance is indicated by the blue text, $\frac{g_m R_o}{1 + g_m R_s}$, which reduces the effective impedance at high frequencies, making $f_H$ larger.
- No Miller effect is indicated by the red text, suggesting that the Miller effect is negligible.

Caltech BSAC
Single Stage Amplifier Cannot Meet All Requirements

• For example, a general purpose operational amplifier requires
  – High input resistance ~ 1MΩ
  – Low output resistance ~ 100Ω
  – High voltage gain ~ 100,000

• No single transistor amplifier can satisfy all spec’s

• Cascading multiple stages of amplifiers offers a path towards the design
Multistage Amplifiers

- Usually
  - An input stage to provide required input resistance
  - Middle stage(s) to provide gain
  - An output stage to provide required output resistance or drive external loads

- More gain!
  - Gain/stage limited, especially in nanoscale devices

- Improve Bandwidth
  - De-couple high impedance nodes from large capacitors

- DC coupling (no passive elements to block the signal)
  - Use amplifiers to naturally “level shift” signal
Biasing

* Discrete

Integrated circuit

DC Biasing
Impedance “Match”

• On-chip circuits often use “voltage/current” matching to minimize loading

• Keep in mind the input resistance and output resistance of each type of stage so that the loading does not create an undesired effect

<table>
<thead>
<tr>
<th></th>
<th>Ideal $R_{in}$</th>
<th>Ideal $R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Amplifier</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Current Amplifier</td>
<td>0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transconductance Amplifier</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transresistance Amplifier</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Two-Stage Voltage Amplifier

- Boost gain by cascading Common-Source stages

Can combine into a single 2-port model
Results of new 2-port:  \( R_{in} = R_{in1}, R_{out} = R_{out2} \)
CS Cascade Analysis

Results of new 2-port:

\[ R_{in} = R_{in1} = \infty \]
\[ R_{out} = R_{out2} = \frac{1}{r_o || r_{oc}} \]
\[ A_V = \frac{v_{out}}{v_{in}} = \frac{1}{g_m v_{int}} \cdot \frac{v_{out}}{v_{int}} = \frac{-g_{m1} \cdot (r_o || r_{oc})}{g_{m2} \cdot (r_o || r_{oc})} \]
\[ \frac{v_{int}}{v_{in}} = \frac{v_{out}}{v_{int}} = \frac{g_{m1}}{g_{m2}} \cdot (r_o || r_{oc})^2. \]
Two time constants:
\[ \tau_1 = \left( C_{gs} + C_m \right) \cdot \frac{1}{\left( r_o \parallel r_{oc} \right) A} \]
\[ \tau_2 = \frac{C_T}{C_m} \]
Bandwidth Extension

- Common Source stage has high gain, but low bandwidth
- Note that Miller effect is the culprit
- Follower stage can buffer source resistance from Miller cap
Bandwidth Extension Using Source Follower (SF)

\[ V_{out} = \frac{V_{in} + V_{int} + V_{int2}}{V_{in}} \cdot \frac{V_{out}}{V_{int}} \cdot \frac{g_{m1}}{g_{m1} (r_o || r_{oc})} \cdot \frac{g_{m2} (r_o || r_{oc})}{r_{o} || r_{oc}} \]
CS Example with Cap Load

- $C_{in}$ and $C_S$ are very large, therefore they look like short circuits to the AC signal.

- If $C_L$ is very large, its pole dominates, let’s analyze...
What are the time constants associated with the capacitors in this circuit?

What can we do if we have to drive a large $C_L$?
• How can we reduce the impact of $C_L$?

• One way is to reduce the resistance $R_d$, but this reduces our low-frequency gain

• To recover the gain we can increase $g_{m1}$.

What does this cost us?
A better way to extend the bandwidth is to add a source-follower stage.

Similar to previous example
By adding a CD (Source Follower) we can increase the bandwidth.

It costs us power for the CD stage.

Remember that increasing the BW by increasing $g_{m1}$ costs us much more.

$$T_2 = C_L \cdot \frac{1}{g_{m2}}$$
CS + CG = Cascode

- Common source provides gain, CG acts as a buffer, but is it even helping?

- How do you bias this circuit?

\[
A_v = -g_m \cdot R_{out} = -g_m (R_I / g_m^2) \\
\approx -g_m \cdot \frac{1}{g_m^2} \approx -1
\]
Merged CS + CG = Cascode

- Let’s apply 2-port small-signal analysis

- In this case, we care about the input current to the second stage

- Note that the input resistance of the CG is low, therefore the majority of the CS current is fed to the CG

- \( A_v = \frac{V_{out}}{V_{in}} = \frac{i_{out}}{i_{in}} \cdot \frac{V_{out}}{V_{in}} = g_m \cdot R_{out} \)
Cascode Bandwidth

• Draw in the $C_{gs}$ and $C_{gd}$ capacitors.
• Which ones are Miller effected?
• Is this better or worse than a CS without a CG?

$$C_m \approx C_{gd}(1 - A)$$

$$C_m = C_{gd}(1 - (-1))$$

$$\approx 2C_{gd}$$
Cascode Bandwidth

• Draw in the capacitors and input resistance

\[ C_M = C_{gd} \left( 1 + \frac{1}{g_{m2}} \right) \]

\[ \approx C_{gd} \left( 1 + \frac{g_{m1}}{g_{m2}} \right) \approx \frac{1}{2} C_{gd} \]
Cascode Biasing

- CG has a very large output resistance
- Loading it with $R_D$ is likely to reduce the voltage gain
- We can increase the gain by using a current source load, but $r_{oc}$ needs to be very large. Can use a cascode current mirror!
Complete Amplifier Design

Goals: \( g_{m1} = 1 \text{ mS} \), \( R_{out} = 5 \text{ M}\Omega \)

For simplicity, let’s assume all \( g_m \) and \( r_o \) values are equal

\[ A_V \approx -g_{m1}R_{out} = -1 \text{ mS} \times 5 \text{ M}\Omega = -5,000 \]

\[ R_{out} \approx \frac{1}{2} g_m r_o^2 = 5 \text{ M}\Omega \]

\[ r_o = \sqrt{\frac{20 \text{ M}\Omega}{g_m}} = \sqrt{\frac{10 \text{ M}\Omega}{1 \text{ mS}}} = 100 \text{k}\Omega \]

\[ A_V = g_{m1} \cdot R_{out} = g_{m1} \cdot g_{m2} \cdot r_o^2 \]
Bias Current & Device Sizing

Need to know process parameters to solve for W/L

\[ k' = 100 \, \mu A/V^2 \]
\[ \lambda = 0.1 \, [V^{-1}] \]

\[ r_o = \frac{1}{\lambda I_{DS}} = 100k\Omega \]
\[ I_{DS} = \frac{1}{0.1V^{-1} \times 100k\Omega} = 100\mu A \]
\[ g_m = \sqrt{2k' \left( \frac{W}{L} \right) I_{DS}} = 1mS \]
\[ \frac{W}{L} = \frac{g_m^2}{2k' I_{DS}} = \frac{(1mS)^2}{2 \times 100\mu \times 100\mu A} = 50 \]
Output (Voltage) Swing

Need to know \( V_{GS} - V_T \) (e.g. \( V_{DSAT}, V_{OV} \))

\[
g_m = \frac{2I_{DS}}{V_{GS} - V_T} = 1mS
\]

\[
V_{GS} - V_T = \frac{2I_{DS}}{g_m} = \frac{2 \times 100 \mu A}{1mS} = 0.2V
\]

Maximum \( V_{OUT} \) = \( V_{DD} - 2V_{sat} = 4.6 \)

Minimum \( V_{OUT} \) = \( 0.4V \),

Input Bias \( V_{IN} \leq 0.7V \).