Multi-Stage Amplifiers
Example of Multi-Stage Amplifier

\[ I_1 = I_2 + I_3 \]

\[ V_{DD} = |V_{gs,p}| + 3|V_{gs,n}| \]

\[ I_S = I_6 \]

\[ V_{bas} \]

\[ |V_{gs,p}| \]

\[ I_{REF} \]

\[ V_{gs,n} \]

\[ \frac{1}{2} R_P (|V_{gs,p}| - |V_{np}|)^2 \]

\[ = \frac{1}{2} R_n (V_{gs,n} - V_{tn})^2 \]
Cutting Through the Complexity

1. Identify the “signal path” between the input and output
2. Eliminate “background” transistors to reduce clutter
3. For “background transistors, understand their role (e.g. DC biasing)
4. For frequency response, identify “hi-Z” nodes.
Eliminate Clutter

\[ V_{DD} - 2|V_{ovp}| \geq V_o \geq V_{ov4} \]

\[ V_{DD} \geq V_o \geq 2V_{ov,n} + 2|V_{ov,p}| \]
Identify Signal Path & Amplifier Stages
DC Biasing

- $V_{B1}$
- $V_{B2}$
- $V_{B3}$

Circuit diagram with transistors M1, M2, M3, and M4, and components $R_S$, $R_L$, $C$, and $V_Q$. The signal $v_s$ is connected to the input, and $v_o$ is the output.
Small-Signal Models

\[ CS + CG = \text{Folded Cascode} \]

\[ R_{o1} = \frac{R_{o1}}{R_{o2}} \]
\[ R_{o3} = g_{m3}R_{o1} \]

\[ V_{in3} = -g_{m2}V_S \]
\[ I_{out} = -V_{in3} = +g_{m2}V_S \]

Without Load: \[ V_{out} = -I_{out}R_{o3} = g_{m2}V_S - g_{m3}R_{o3}(R_{o1}/R_{o2}) \]
Two-Port Model

\[
A_v = \frac{g_{m2} g_{m3} R_0}{(R_0 || R_2)}
\]

**Transconductance**

\[
R_{01} = R_{02} \parallel R_0 \Rightarrow \frac{1}{g_{m3}}
\]

\[
R_{03} = \left[\frac{g_{m3} (R_0 || R_2)}{R_0} \right] \parallel R_{04} \parallel R_L
\]

\[
I_c = (-g_{m2} V_c)
\]

\[
V_{out} = -I_c \cdot R_{03} \times (-1)
\]

\[
R_{03} (1 + g_{m3} (R_0 || R_2)) \approx R_{03} \cdot g_{m3} (R_0 || R_2)
\]
External Loads

- Many applications must drive external loads that are very low impedance compared to on-chip levels.
- These stages must drive high voltages/currents so linearity is a concert. We must consider “large signal” behavior.
- Example: Speaker at 8 ohms versus Megaohms on-chip ...
- Follower is natural choice, but it can only “source” current (think in terms of large signals).
Design Issue: DC Coupling

• Constraint: large inductors and capacitors are not available

• Output of one stage is directly connected to the input of the next stage → must consider DC levels … why?