EE105 – Fall 2015
Microelectronic Devices and Circuits
Module 4-5: Differential Amplifiers

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Signal ← noise, background

\[ V_{\text{out}} = V_{\text{in1}} - V_{\text{in2}} \]

Output is insensitive common mode signal

\[ V_{\text{gs1}} = V_{\text{gs2}} \text{ always} \]

\[ I_{\text{d1}} + I_{\text{d2}} = I_{\text{d}} \]

\[ I_{\text{d1}} = I_{\text{d2}} = \frac{I_{\text{d}}}{2} \]

Common mode: \( V_{\text{id}} = 0 \)

Differential signal \( \frac{I_{\text{d}}}{2} + i \downarrow \frac{I_{\text{d}}}{2} - i \)

Virtual ground for small-signal differential mode

\[ V_{\text{A}} \cdot V_{\text{B}} \Rightarrow V_{\text{A}} = \frac{V_{\text{A}} + V_{\text{B}}}{2} + \frac{V_{\text{A}} - V_{\text{B}}}{2} = V_{\text{cm}} + \frac{V_{\text{id}}}{2} \]

\[ V_{\text{B}} = \frac{V_{\text{A}} + V_{\text{B}}}{2} - \frac{V_{\text{A}} - V_{\text{B}}}{2} = V_{\text{cm}} - \frac{V_{\text{id}}}{2} \]
Half Circuit

\[ V_{\text{dd}} \]

\[ V_{\text{dd}} \]

\[ V_{\text{dd}} \]

\[ \frac{V_{\text{dd}}}{2} \]

\[ \frac{V_{\text{dd}}}{2} \]

\[ \Rightarrow \text{common source} \]

\[ V_{gs1} = \frac{V_{\text{dd}}}{2} \]

\[ V_{o1} = -g_m \left( \frac{V_{\text{dd}}}{2} \right) R_D \]

\[ V_{o2} = -g_m \left( -\frac{V_{\text{dd}}}{2} \right) R_D \]

\[ V_{os} = V_{o1} - V_{o2} = -g_m R_D \cdot V_{\text{dd}} \]

\[ A_D = \frac{V_{os}}{V_{\text{dd}}} = -g_m R_D \]

\[ \uparrow \text{same as CS Amp} \]

Common Mode: Left and Right are symmetric

\[ V_{\text{dd}} \]

\[ V_{\text{cm}} \]

\[ V_{\text{cm}} \]

\[ I_D \]

\[ \frac{V_{\text{os}}}{R_{ss}} (= R_o) \]

\[ AC \]
CM equivalent net is CS with source degeneration

\[ V_{o1} = V_{o2} \quad \Rightarrow \quad V_{o2} = V_{o1} - V_{d} = 0 \]

Ideal matching

\[ R_{D1} = R_{D2} = R_{D} \]
\[ g_{m1} = g_{m2} = g_{m} \]

\[ U_{g/s} = U_{CM} - (g_{m} U_{g/s}) \cdot 2R_{ss} \]

\[ U_{g/s} = \frac{U_{CM}}{1 + g_{m} 2R_{ss}} \]

\[ V_{o1} = -i \cdot R_{D} = -g_{m} \frac{U_{CM}}{1 + g_{m} 2R_{ss}} \cdot R_{D} \]

\[ A_{V1} = \frac{V_{o1}}{U_{CM}} = -\frac{g_{m} R_{D}}{1 + g_{m} 2R_{ss}} = -\frac{R_{D}}{\frac{1}{g_{m}} + 2R_{ss}} \approx -\frac{R_{D}}{2R_{ss}} \]

\[ R_{ss} \sim R_{D} \gg \frac{1}{g_{m}} \]

\[ \therefore \quad \pi_{m} \approx \pi_{m} \]
Differential “Half Circuit”

\[ A_{CM} = \frac{1}{2} \frac{v_{od}}{v_{CM}} = 0 \]

Because the two halves of the circuits are anti-symmetric, and Source is at virtual ground, we can simplified and just analyze the "half circuit"
Ideal CM Output Voltage

The common-mode half-circuit is basically a common-source amplifier with source degeneration.

The gain is

\[ \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{1/g_m + 2R_{SS}} \]

Since \( 2R_{SS} >> 1/g_m \),

\[ \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \approx -\frac{R_D}{2R_{SS}} \]

\[ v_{od} = v_{o2} - v_{o1} = 0 \]

Output voltage is zero for ideal differential pair with perfectly matched transistors and resistors, and the CM voltage is small enough that \( Q_1 \) and \( Q_2 \) remains in Saturation.

Common-Source with degeneration

Biased at \( I/2 \)
Common Mode Gain with Mismatched $R_D$

However, any mismatch in the half circuits will produce finite output voltage, e.g.,

$$R_{D2} = R_D + \Delta R_D$$

$$v_{od} = v_{o2} - v_{o1} = \frac{-\Delta R_D}{2R_{SS}} v_{icm}$$

Common mode gain:

$$A_{cm} = \frac{v_{od}}{v_{icm}} = \frac{-\Delta R_D}{2R_{SS}} = \left(\frac{-R_D}{2R_{SS}}\right) \left(\frac{\Delta R_D}{R_D}\right)$$

Common Mode Rejection Ratio (CMRR):

$$CMRR \equiv \left| \frac{A_d}{A_{cm}} \right| , \quad \text{in dB: } CMRR(dB) \equiv 20 \log \left(\frac{|A_d|}{|A_{cm}|}\right)$$

CMRR should be as large as possible.

For the above case,

$$CMRR = \frac{g_m R_D}{\Delta R_D} = \frac{2g_m R_{SS}}{\left(\frac{\Delta R_D}{R_D}\right)}$$

Typical ex. $R_{SS} \sim R_D$; $R_D \sim 100 \cdot \frac{1}{g_m}$

$\frac{\Delta R_D}{R_D} = 1\%$

$$CMRR = \frac{200}{1\%} = 2 \times 10^4$$

$$20 \log (2 \times 10^4) = 140 \text{ dB}$$
Common Mode Gain with Mismatch of $g_m$

Mismatch in $g_m$:

$$g_{m1} = g_m + \frac{1}{2} \Delta g_m; \quad g_{m2} = g_m - \frac{1}{2} \Delta g_m$$

$$g_{m1} - g_{m2} = \Delta g_m$$

(Derivation skipped)

$$A_{cm} = \frac{v_{od}}{v_{icm}} = \left( \frac{R_D}{2R_{SS}} \right) \frac{\Delta g_m}{g_m}$$

$$CMRR = \frac{g_m R_D}{2R_{SS} g_m} = \frac{2g_m R_{SS}}{\left( \frac{\Delta g_m}{g_m} \right)}$$

$$\times V_{o1} = -\frac{R_D}{2R_{SS}} \rightarrow V_{o1} = -\frac{R_D}{\left( \frac{1}{g_m} + \frac{1}{2\Delta g_m} \right) + 2R_{SS}}$$

$$V_{o2} = -\frac{R_D}{\left( \frac{1}{g_m} - \frac{1}{2\Delta g_m} \right) + 2R_{SS}}$$

$$\Rightarrow V_{od} = V_{o2} - V_{o1}$$
Add offset voltage to "null" the $V_{0d}$

Due to mismatch in $R_D$, output voltage $V_O \neq 0$ even both inputs are grounded. To produce zero output, an input offset voltage

$V_{OS} = \frac{V_O}{A_d}$, where $A_d$ is differential gain, needs to be applied.

$V_O = A_d \cdot V_{OS} = (g_m R_D) \cdot V_{OS} \Rightarrow V_{OS} = \frac{V_O}{A_d} = \frac{V_O}{g_m R_D}$
DC Offset

For example, DC offset caused by mismatch in $R_D$:

$$R_{D1} = R_D + \frac{\Delta R_D}{2};$$
$$R_{D2} = R_D - \frac{\Delta R_D}{2};$$
$$V_O = V_{D2} - V_{D1} = \frac{I}{2} \Delta R_D$$

$$V_{OS} = \frac{V_O}{A_d} = \frac{I \Delta R_D / 2}{g_m R_D} = \frac{\Delta R_D / 2}{2 \left( \frac{I}{2 V_{OV}} \right) R_D} = \left( \frac{V_{OV}}{2} \right) \left( \frac{\Delta R_D}{2} \right) R_D$$
Useful Metric for Diff Amps: CMRR

**Common Mode Rejection Ratio (CMRR)**
- Define: $a_{vd}$: differential gain, $a_{vc}$: common mode gain

$$CMRR = \left( \frac{a_{vd}}{a_{vc}} \right)$$

- CMRR corresponds to ratio of differential to common mode gain and is related to received signal-to-noise ratio

$$V_{od} = a_{vd} V_{sig} + a_{vc} V_{noise}$$

$$\Rightarrow \frac{Signal}{Noise} = \left( \frac{a_{vd}}{a_{vc}} \right) \left( \frac{V_{sig}}{V_{noise}} \right) = CMRR \left( \frac{V_{sig}}{V_{noise}} \right)$$

Courtesy: M.H. Perrott
Differential Amplifier with Current-Source Loads

\[ A_d = \frac{V_{od}}{V_{id}} = g_{m1} \left( r_{o1} \parallel r_{o3} \right) \]

\( Q_3 \) and \( Q_4 \) are PMOS current sources (active loads)

From half-circuit
Cascode Differential Amplifier

Cascode configurations for both amplifying transistors and current source loads.

From half-circuit

\[ A_d = \frac{v_{od}}{v_{id}} = g_{m1} \left( R_{on} \parallel R_{op} \right) \]

\[ R_{on} = (g_{m3}r_{o3})r_{o1} \]

\[ R_{op} = (g_{m5}r_{o5})r_{o7} \]

If all transistors are identical,

\[ R_{on} = R_{op} = g_mr_{o}^2 \]

\[ A_d = \frac{1}{2} g_m^2 r_{o}^2 \]
Differential Input, Single-End Output

Differential-in, Differential-out

Differential input, Single-ended Output
MOS Differential Pair with Current Mirror Load

AC equivalent circuit for differential input

Current mirror forces small-signal currents through Q₃ and Q₄ to be the same → output currents = 2x that of half circuit