Two-Stage CMOS Op-Amp Circuit
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- Current Mirrors
- Differential Pair with Current Mirror Load
- Common Source Amplifier Stage

Diagram includes transistors and labels for each component.
Two-Stage CMOS Op-Amp Circuit

Voltage gain of the first stage (Q₁, Q₂): Differential input, single-ended output:

\[ A_1 = -g_{m1} \left( r_{o2} \parallel r_{o4} \right) \]

Voltage gain of the 2nd stage (Q₆): Common source with current source load:

\[ A_2 = -g_{m6} \left( r_{o6} \parallel r_{o7} \right) \]

Total gain

\[ A_o = A_1 A_2 \]
Example:

<table>
<thead>
<tr>
<th></th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L</td>
<td>20/0.8</td>
<td>20/0.8</td>
<td>5/0.8</td>
<td>5/0.8</td>
</tr>
<tr>
<td>in um</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Q5</th>
<th>Q6</th>
<th>Q7</th>
<th>Q8</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L</td>
<td>40/0.8</td>
<td>10/0.8</td>
<td>4/0.8</td>
<td>4/0.8</td>
</tr>
<tr>
<td>in um</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

I_{REF} = 90 \mu A, \ V_{tn} = 0.7V, \ V_{tp} = -0.8V
\mu_nC_{ox} = 160 \mu A/V^2, \mu_pC_{ox} = 40 \mu A/V^2
|VA| = 10V for all devices
V_{DD} = V_{SS} = 2.5V

Find I_D, |V_{OVL}|, |V_{GS}|, g_m, r_o for all Q’s, voltage gain, input common mode range, output voltage range.
Solution: DC Parameters

\( I_{REF} = 90 \mu A \)

\( I_{D5} = \frac{(W/L)_5}{(W/L)_8} = 90 \mu A \)

\( I_{D7} = \frac{(W/L)_7}{(W/L)_8} = 90 \mu A \)

\( I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D5}}{2} = 45 \mu A \)

\( I_{Di} = \frac{1}{2} \mu_i C_{ox} \left( \frac{W}{L} \right) |V_{OV}|^2 \)

\( |V_{OV1}| = |V_{OV2}| = |V_{OV3}| = |V_{OV4}| = 0.3 \)

\( |V_{OV5}| = |V_{OV6}| = |V_{OV7}| = |V_{OV8}| = 0.3 \)

\( |V_{GS}| = |V_{OV}| + |V_t| \)

NMOS: \( |V_{GS}| = 0.3 + 0.7 = 1.0V \)

PMOS: \( |V_{GS}| = 0.3 + 0.8 = 1.1V \)
Solution: AC Parameters

\[ g_m = \frac{2I_D}{|V_{OV}|} \]

\[ g_{m1-4} = 2 \times 45 \mu A / 0.3V = 0.3mA / V \]
\[ g_{m5-8} = 2 \times 90 \mu A / 0.3V = 0.6mA / V \]

\[ r_o = \frac{|V_A|}{I_D} \]

\[ r_{o1-4} = \frac{10V}{45 \mu A} = 222k\Omega \]
\[ r_{o5-8} = \frac{10V}{90 \mu A} = 111k\Omega \]

\[ A_1 = -g_{m1}(r_{o2} \parallel r_{o4}) \]
\[ = -0.3 \times 222 / 2 = -33.3V / V \]

\[ A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \]
\[ = -0.6 \times 111 / 2 = -33.3V / V \]

\[ A_o = A_1A_2 = 1109V / V \]
\[ = 20 \log(1109) = 61dB \]
Solution: Input Common-Mode Ranges

Input common-mode voltage range:
Maximum: \( Q_5 \) near edge of saturation

\[
|V_{DS5}| = |V_{OV5}| = 0.3V
\]

\[
\nu_{icm}^{\text{max}} = 2.5 - |V_{OV5}| - |V_{GS5}|
\]

\[
= 2.5 - 0.3 - 1.1 = 1.1V
\]

Minimum: \( Q_1 \) near edge of saturation

\[
\nu_{D1} = -V_{SS} + V_{GS3} = -2.5 + 1 = -1.5V
\]

\[
|\nu_{DS1}| = |\nu_{GS1}| - |\nu_{ip}|
\]

\[
-\nu_{DS1} = -\nu_{GS1} - 0.8
\]

\[
-\nu_{D1} = -\nu_{G1} - 0.8
\]

\[
\nu_{icm}^{\text{min}} = \nu_{G1} = \nu_{D1} - 0.8 = -2.3V
\]
Output voltage range:

Maximum: $Q_7$ near edge of saturation

$$|V_{OV7}| = 0.3V$$

$$v_{o_{max}} = 2.5 - |V_{OV7}| = 2.2V$$

Minimum: $Q_6$ near edge of saturation

$$v_{o_{min}} = -V_{SS} + |V_{OV6}| = -2.5 + 0.3 = -2.2V$$
Folded-Cascode CMOS Op Amp.
(for inspection only)
741 Op-Amp Circuit

Reference current

First stage

$V_{CC} (+15 \text{ V})$

Second stage

Output stage

$R_5 = 39 \text{ k}\Omega$

$I_{REF}$

$-V_{EE} (-15 \text{ V})$

$Q_{12}$

$Q_{11}$

$Q_{10}$

$Q_{9}$

$Q_{8}$

$Q_1$

$Q_2$

$Q_3$

$Q_4$

$Q_6$

$Q_5$

$Q_7$

$Q_{13A}$

$Q_{13B}$

$Q_{14}$

$Q_{15}$

$Q_{16}$

$Q_{17}$

$Q_{18}$

$Q_{19}$

$Q_{20}$

$Q_{21}$

$Q_{22}$

$Q_{23}$

$Q_{24}$

$R_4 = 5 \text{ k}\Omega$

$R_3 = 50 \text{ k}\Omega$

$R_2 = 1 \text{ k}\Omega$

$R_1 = 1 \text{ k}\Omega$

$C_c = 30 \text{ pF}$

$R_9 = 50 \text{ k}\Omega$

$R_8 = 100 \text{ \Omega}$

$R_7 = 27 \text{ \Omega}$

$R_6 = 27 \text{ \Omega}$

Out
Functions of Various Transistors

• $Q_{11}, Q_{12},$ and $R_5$ generate a reference bias current, $I_{\text{REF}}$.

• $Q_{10}, Q_{9},$ and $Q_8$ bias the input stage, which is composed of $Q_1$ to $Q_7$.

• The second gain stage is composed of $Q_{16}$ and $Q_{17}$ with $Q_{13B}$ acting as active load.

• The class AB output stage is formed by $Q_{14}$ and $Q_{20}$ with biasing devices $Q_{13A}, Q_{18},$ and $Q_{19}$, and an input buffer $Q_{23}$.

• Transistors $Q_{15}, Q_{21}, Q_{24},$ and $Q_{22}$ serve to protect the amplifier against output short circuits and are normally cut off.