EE 105 | Final Review

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Outline

• Exercise 1
  – Op-Amp
  – Feedback
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• Exercise 2
  – Semiconductor physics
• Exercise 3
  – Device structures and operation
    • BJT & MOSFET
  – Large signal operation (DC operating point)
  – Small signal operation
Outline

• Exercise 4
  – Multi-stage amplifier analysis
    • Inspection analysis
    • Miller effect
    • Mid-band gain
    • High corner frequency (OCTC)
    • Low corner frequency (SCTC)
    • Small-signal limitation and output swing

• Exercise 5
  – Differential pair analysis

• Digital circuit overview and CMOS logic circuit design
Exercise 1 – Ideal Op-amps

- Ideal Op-amp laws
  1. $R_{\text{in}} = \infty$
  2. $R_{\text{out}} = 0$
  3. $A_v = \infty$

\[ V_o = A_v (v^+ - v^-) \]

$\Rightarrow V_o = 0 \Rightarrow v^+ = v^-$ only in negative FB
Exercise 1 – Basic Op-amp Configurations

1. Inverting Amplifier

\[ \frac{v_o}{v_i} = -\frac{R_2}{R_1} \]

2. Non-inverting Amplifier

\[ \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1} \]

3. Integrating Amplifier

\[ i_i = \frac{v_i}{R}; \quad v_o = 0 - i_i \frac{1}{sC} \]
\[ v_o = -\frac{v_i}{sRC} \Rightarrow \frac{v_i}{v_i} = -\frac{1}{sRC} \]

DC gain is 0

\[ \omega_p = \frac{1}{RC} \]

20dB/dec
Exercise 1 – Op-amp Nonidealities

Input offset voltage

\[ v_{\text{os}} = \frac{v_{\text{os}} - v_{\text{os}}}{R_1} = \frac{-v_{\text{os}}}{R_1} \]

\[ v_{\text{in}} = v_{\text{in}} - v_{\text{os}} = \frac{-v_{\text{os}}}{R_1} \]

\[ v_o = v_{\text{os}} - v_{\text{in}}R_2 = v_{\text{os}} + \frac{R_2}{R_1}v_{\text{os}} \]

How to find/measure \( v_{\text{os}} \)?

Ground input & measure \( v_o \).

\[ v_{\text{in}} = v_{\text{os}} - v_{\text{os}} = v_{\text{os}} \]

\[ v_o = v_{\text{os}} + \frac{R_2}{R_1}v_{\text{os}} \]

Get this from measure \( v_o \)
Exercise 1 – Op-amp Nonidealities

Finite Gain

\[ A_v \neq \infty \text{ (open loop gain)} \]

\[ v_o = A_v (v^+ - v^-) = -A_v v^- \]

\[ i_{in} = \frac{v_{in} - v^-}{R_1} = \frac{v^- - v_o}{R_2} \]

\[ \frac{R_2}{R_1} \left( v_{in} + \frac{v_o}{A_v} \right) = -v_o \left( 1 + \frac{1}{A_v} \right) \]

\[ \frac{v_o}{v_i} = \left| \frac{-R_2/R_1}{1 + \frac{R_2/R_1 + 1}{A_v}} \right| < \left| -\frac{R_2}{R_1} \right| \]

\[ \text{closed-loop gain if } A_v \to \infty \]

\[ A_v \to \infty \Rightarrow \frac{v_o}{v_i} = -\frac{R_2}{R_1} \]
Exercise 1 – Op-amp Nonidealities

Input Bias Current (& Offset)

\[ R_1 \parallel R_2 \text{ to eliminate effects of } \]

\[ \text{nonideal} \]

\[ \begin{align*}
I_0 & = 0 \\
R_1 & = 0.1I_0 \\
R_2 & = \text{measure for } v_{\text{in}} = 0 \text{ V} \\
R_b & \text{ means for no-offset case, } v_o = 0 \\
\end{align*} \]

Say we have 10\% I_{bias} offset...

\[ v_o = (0.1I_b)R_2 \]
Exercise 1 – Frequency Response & Bode Plots

Generic 1 & 2-pole systems

\[ |H(s)| = \frac{-A_{dc}}{1 + \frac{s}{\omega_p}} \]

\[ \angle H(s) = -A_{dc} \left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right) \]
Exercise 2 – Semiconductor Physics

N & P-Type Semiconductors

\[ \text{acceptors ("accept" } e^- \rightarrow h^+) \left[ N_A \text{ cm}^{-3} \right] \]

\[ \text{dopants are donors ("donate" } e^-) \left[ N_0 \text{ cm}^{-3} \right] \]
Exercise 2 – Semiconductor Physics

PN Junctions

\[ Q_p = Q_N = \int (N, \text{Volume}) \]

\[ P \rightarrow N \]

\[ P \rightarrow W_p \]

\[ N \rightarrow W_N \]
Exercise 2 – Semiconductor Physics

PN Junctions with external energy

- Fixed charge region
- Drift current due to $e^-$ swept across depletion region
- Diffusion of $h^+$ due to conc. grad.
- "Just outside of fixed chg. reg."
- Laser creating $e^-/h^+$ pairs
- $R_{load}$
Exercise 3

- Device structures and operation
  - BJT & MOSFET
  - Large signal operation (DC operating point)
  - Small signal operation

Regions of operation:
Exercise 3

- Large signal operation (DC operating point)

\[ V = +18 \text{ V} \]

\[ M_1 \]

\[ R_1 = 500 \text{ k}\Omega \]
\[ R_2 = 75 \text{ k}\Omega \]
\[ R_3 = 1.4 \text{ M}\Omega \]
\[ R_4 = 27 \text{ k}\Omega \]

- Assume in saturation
- Solve for the drain current
- Check the assumption
- **If not in saturation, assume in linear region**
- Solve for the drain current
- Check the assumption
- If not in linear region, M1 is cut-off
Exercise 3

- Generate small signal model @ $V_{in} = 1V$

\[ I_{in} \propto V_{in}^2 \]
\[ I_{out} \propto V_{in}^2 \]
\[ I_{out} \propto (2V)^2 \]

\[ I = 0.005V^2 + 0.005V \]
\[ I = 0.001V^2 + 0.004V \]
\[ I = 0.001\sin(2V) \]
Exercise 4

- Exercise 4
  - Multi-stage amplifier analysis
    - Inspection analysis
    - Miller effect
    - Mid-band gain
    - High corner frequency (OCTC)
    - Low corner frequency (SCTC)
    - Small-signal limitation and output swing
4. For the amplifier in Figure PS10.3, assume that $M_1$ has the properties listed in Table PS10.2, and that $Q_1$ has the properties listed in Table PS10.1. Find $A_v\left(\frac{v_{out}}{v_s}\right)$, $R_{in}$, $R_{out}$, $f_L$, and $f_H$. 

![Circuit Diagram](image-url)
4. For the amplifier in Figure PS10.3, assume that $M_1$ has the properties listed in Table PS10.2, and that $Q_3$ has the properties listed in Table PS10.1. Find $A_v$, $R_{in}$, $R_{out}$, $f_s$, and $f_h$. 

Figure PS10.3
Exercise 5

- Find $A_{v,d}$, $A_{v,c}$, and **CMRR**

![Circuit Diagram](image.png)
Exercise 5

- Find $A_{v,d}, A_{v,c}$, and **CMRR**

![Figure P9.128](image-url)
Exercise 5

• Find $A_{v,d}, A_{v,c},$ and **CMRR**

![Figure P9.128](image-url)
Digital circuit overview

- Digital circuit component
  - Inverter
  -Latch
  - Flip-flop
  - Pass-gate
  - …
Digital circuit overview

- Ring Oscillator
Digital circuit overview

- CMOS logic