Consider a transistor biased to operate in the active mode at a dc collector current \(I_C\). Calculate the collector signal current as a fraction of \(I_C\) (i.e., \(i_c/I_c\)) for input signals \(v_m\) of +1 mV, -1 mV, +2 mV, -2 mV, +5 mV, -5 mV, +8 mV, -8 mV, +10 mV, -10 mV, +12 mV, and -12 mV. In each case do the calculation two ways:

(a) using the exponential characteristic, and
(b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

An npn BJT with grounded emitter is operated with \(V_{BE} = 0.700\) V, at which the collector current is 0.5 mA. A 5-kΩ resistor connects the collector to a +5-V supply. What is the resulting collector voltage \(V_C\)? Now, if a signal applied to the base raises \(v_{BE}\) to 705 mV, find the resulting total collector current \(i_c\) and total collector voltage \(v_C\) using the exponential \(i_C = v_C/R_C\) relationship. For this situation, what are \(v_{m}\) and \(v_C\)? Calculate the voltage gain \(v_C/v_m\). Compare with the value obtained using the small-signal approximation, that is, \(-g_m R_C\).

A transistor with \(\beta = 100\) is biased to operate at a dc collector current of 0.5 mA. Find the values of \(g_m\), \(r_n\), and \(r_e\). Repeat for a bias current of 50 μA.

A pnp BJT is biased to operate at \(I_C = 1.0\) mA. What is the associated value of \(g_m\)? If \(\beta = 100\), what is the value of the small-signal resistance seen looking into the emitter \((r_e)\)? Into the base \((r_n)\)? If the collector is connected to a 5-kΩ load, with a signal of 5-mV peak applied between base and emitter, what output signal voltage results?

A designer wishes to create a BJT amplifier with a \(g_m\) of 30 mA/V and a base input resistance of 3000 Ω or more.

What collector-bias current should he choose? What is the minimum \(\beta\) he can tolerate for the transistor used?

A transistor operating with nominal \(g_m\) of 40 mA/V has a \(\beta\) that ranges from 50 to 150. Also, the bias circuit, being less than ideal, allows a ±20% variation in \(I_C\). What are the extreme values found of the resistance looking into the base?

In the circuit of Fig. 7.20, \(V_{BE}\) is adjusted so that \(V_C = 1\) V. If \(V_{CC} = 3\) V, \(R_C = 2\) kΩ, and a signal \(v_m = 0.005\) sin \(\omega t\) volts is applied, find expressions for the total instantaneous quantities \(i_c(t)\), \(v_C(t)\), and \(i_B(t)\). The transistor has \(\beta = 100\). What is the voltage gain?

We wish to design the amplifier circuit of Fig. 7.20 under the constraint that \(V_{CC}\) is fixed. Let the input signal \(v_m = \tilde{V}_m\) sin \(\omega t\), where \(\tilde{V}_m\) is the maximum value for acceptable linearity. For the design that results in the largest signal at the collector, without the BJT leaving the active region, show that

\[
R_C I_C = (V_{CC} - 0.3) / \left(1 + \frac{\tilde{V}_m}{V_T}\right)
\]

and find an expression for the voltage gain obtained. For \(V_{CC} = 3\) V and \(\tilde{V}_m = 5\) mV, find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

The table below summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifiers under various conditions. Provide the missing entries. (Note: Isn’t it remarkable how much two parameters can reveal?)

A BJT is biased to operate in the active mode at a dc collector current of 1 mA. It has a \(\beta\) of 100 and \(V_A\) of 100 V. Give the four small-signal models (Figs. 7.25 and 7.27) of the BJT complete with the values of their parameters.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>a</th>
<th>b</th>
<th>c</th>
<th>d</th>
<th>e</th>
<th>f</th>
<th>g</th>
</tr>
</thead>
<tbody>
<tr>
<td>α</td>
<td>1.00</td>
<td>100</td>
<td>1.00</td>
<td>∞</td>
<td>0.90</td>
<td>5</td>
<td>1.10</td>
</tr>
<tr>
<td>β</td>
<td>1.00</td>
<td>1.00</td>
<td>0.020</td>
<td>25</td>
<td>100</td>
<td>700</td>
<td></td>
</tr>
<tr>
<td>(I_C) (mA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_E) (mA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(g_m) (mA/V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(r_e) (Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(r_n) (Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem**
than 10 mV). Find appropriate values for $R_e$ and $R_C$. What is the value of voltage gain realized from signal source to output?

**7.58** The transistor in the circuit shown in Fig. P7.58 is biased to operate in the active mode. Assuming that $\beta$ is very large, find the collector bias current $I_C$. Replace the transistor with the small-signal equivalent-circuit model of Fig. 7.26(b) (remember to replace the dc power supply with a short circuit). Analyze the resulting amplifier equivalent circuit to show that

\[
\frac{v_{o1}}{v_i} = \frac{R_e}{R_e + r_e}
\]

\[
\frac{v_{o2}}{v_i} = \frac{-\alpha R_C}{R_e + r_e}
\]

Find the values of these voltage gains (for $\alpha \simeq 1$). Now, if the terminal labeled $v_{o1}$ is connected to ground, what does the voltage gain $v_{o1}/v_i$ become?

**7.59** An amplifier with an input resistance of 100 kΩ, an open-circuit voltage gain of 100 V/V, and an output resistance of 100 Ω is connected between a 20-kΩ signal source and a 2-kΩ load. Find the overall voltage gain $G_v$. Also find the current gain, defined as the ratio of the load current to the current drawn from the signal source.

**7.60** Specify the parameters $R_{in}$, $A_{ve}$, and $R_e$ of an amplifier that is to be connected between a 100-kΩ source and a 2-kΩ load and is required to meet the following specifications:

(a) No more than 5% of the signal strength is lost in the connection to the amplifier input;

(b) If the load resistance changes from the nominal value of 2 kΩ to a low value of 1 kΩ, the change in output voltage is limited to 5% of nominal value; and

(c) The nominal overall voltage gain is 10 V/V.

**7.61** Figure P7.61 shows an alternative equivalent-circuit representation of an amplifier. If this circuit is to be equivalent to that in Fig. 7.34(b) show that $G_m = A_{ve}/R_e$. Also convince yourself that the transconductance $G_m$ is defined as

\[
G_m = \left. \frac{i_v}{v_i} \right|_{R_L = 0}
\]

and hence is known as the short-circuit transconductance. Now, if the amplifier is fed with a signal source $(v_{sig}, R_{sig})$ and is connected to a load resistance $R_L$, show that the gain of the amplifier proper $A_v$ is given by $A_v = G_m (R_e || R_L)$ and the overall voltage gain $G_v$ is given by

\[
G_v = \frac{R_{in}}{R_{in} + R_{sig}} G_m (R_e || R_L)
\]

**7.62** An alternative equivalent circuit of an amplifier fed with a signal source $(v_{sig}, R_{sig})$ and connected to a load $R_L$ is shown in Fig. P7.62. Here $G_{ve}$ is the open-circuit overall voltage gain,

\[
G_{ve} = \left. \frac{v_o}{v_{sig}} \right|_{R_L = \infty}
\]

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SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem
(b) Show that including $R_c$ reduces the magnitude of $A_m$ by a certain factor. What is this factor?
(c) Show that including $R_c$ reduces $f_l$ by the same factor as in (b) and thus one can use $R_c$ to trade off gain for bandwidth.
(d) For $I = 0.25$ mA, $R_c = 10$ kΩ, and $C_e = 10$ µF, find $|A_m|$ and $f_l$ with $R_c = 0$. Now find the value of $R_c$ that lowers $f_l$ by a factor of 10. What will the gain become? Sketch on the same diagram a Bode plot for the gain magnitude for both cases.

Section 10.2: Internal Capacitive Effects and the High-Frequency Model of the MOSFET and the BJT

10.13 Refer to the MOSFET high-frequency model in Fig. 10.12(a). Evaluate the model parameters for an NMOS transistor operating at $I_D = 200$ µA, $V_{GB} = 1$ V, and $V_{DS} = 1.5$ V. The MOSFET has $W = 20$ µm, $L = 1$ µm, $r_{as} = 8$ nm, $\mu_n = 450$ cm$^2$/V·s, $\gamma = 0.5$ V$^{1/2}$, $2\phi_F = 0.65$ V, $\lambda = 0.05$ V$^{-1}$, $V_T = 0.7$ V, $C_{so} = C_{do} = 20$ fF, and $L_{ov} = 0.05$ µm. [Recall that $g_{ms} = \chi g_{ns}$, where $\chi = \gamma/(2\sqrt{2\phi_F + V_{gs}}), and that $e_{ns} = 3.45 \times 10^{-11}$ F/m.]

10.14 Find $f_T$ for a MOSFET operating at $I_D = 200$ µA and $V_{OV} = 0.3$ V. The MOSFET has $C_{gs} = 25$ fF and $C_{sd} = 5$ fF.

10.15 Starting from the expression of $f_T$ for a MOSFET,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{sd})}$$

and making the approximation that $C_{gs} \gg C_{sd}$ and that the overlap component of $C_{gs}$ is negligibly small, show that

$$f_T \approx \frac{1}{2\pi L} \sqrt{\frac{\mu_n J_D}{2C_{mn} W L}}$$

Thus note that to obtain a high $f_T$ from a given device, it must be operated at a high current. Also note that faster operation is obtained from smaller devices.

10.16 Starting from the expression for the MOSFET unity-gain frequency,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{sd})}$$

and making the approximation that $C_{gs} \gg C_{sd}$ and that the overlap component of $C_{gs}$ is negligibly small, show that for an $n$-channel device

$$f_T \approx \frac{3\mu_n V_{OV}}{4\pi L^2}$$

Observe that for a given channel length, $f_T$ can be increased by operating the MOSFET at a higher overdrive voltage. Evaluate $f_T$ for devices with $L = 0.5$ µ m operated at overdrive voltages of 0.2 V and 0.4 V. Use $\mu_n = 450$ cm$^2$/V·s.

10.17 It is required to calculate the intrinsic gain $A_0$ and the unity-gain frequency $f_T$ of an $n$-channel transistor fabricated in a 0.13-µm CMOS process for which $L_{ov} = 0.1$ µ m, $\mu_n = 400$ cm$^2$/V·s, and $V_T = 5$ V/µm. The device is operated at $V_{OV} = 0.2$ V. Find $A_0$ and $f_T$ for devices with $L = L_{min}$, $2L_{min}$, $3L_{min}$, $4L_{min}$, and $5L_{min}$. Present your results in a table. (Hint: For $f_T$, use the approximate expression $f_T \approx \frac{3\mu_n V_{OV}}{4\pi L^2}$.)

10.18 A particular BJT operating at $I_C = 0.5$ mA has $C_e = 1$ pF, $C_o = 8$ pF, and $\beta = 100$. What are $f_T$ and $f_p$ for this situation?

10.19 For the transistor described in Problem 10.18, $C_t$ includes a relatively constant depletion-layer capacitance

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$I_D$ (mA)</th>
<th>$r_e$(Ω)</th>
<th>$g_m$(mAV)</th>
<th>$r_s$(kΩ)</th>
<th>$\beta_0$</th>
<th>$f_T$(MHz)</th>
<th>$C_e$(pF)</th>
<th>$C_o$(pF)</th>
<th>$f_p$(MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>2</td>
<td>25</td>
<td>2.5</td>
<td>100</td>
<td>500</td>
<td>2</td>
<td>10.7</td>
<td>9</td>
<td>80</td>
</tr>
<tr>
<td>(b)</td>
<td>10</td>
<td>0.1</td>
<td>800</td>
<td>100</td>
<td>150</td>
<td>2</td>
<td>10.7</td>
<td>9</td>
<td>80</td>
</tr>
<tr>
<td>(c)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>100</td>
<td>500</td>
<td>2</td>
<td>10.7</td>
<td>9</td>
<td>80</td>
</tr>
</tbody>
</table>

* = difficult problem; ** = more difficult; *** = very challenging; D = design problem
of 2 pF. If the device is operated at $I_c = 0.25$ mA, what does its $f_r$ become?

10.20 An npn transistor is operated at $I_c = 1$ mA and $V_{ce} = 2$ V. It has $\beta_0 = 100$, $V_A = 50$ V, $\tau_f = 30$ ps, $C_{je} = 20$ fF, $C_{re} = 30$ fF, $V_{oc} = 0.75$ V, $m_{cm} = 0.5$, and $r_s = 100$ $\Omega$. Sketch the complete hybrid-$\pi$ model, and specify the values of all its components. Also, find $f_r$.

10.21 Measurement of $h_{fe}$ of an npn transistor at 50 MHz shows that $|h_{fe}| = 10$ at $I_c = 0.2$ mA and 12 at $I_c = 1.0$ mA. Furthermore, $C_{c's}$ was measured and found to be 0.1 pF. Find $f_r$ at each of the two collector currents used. What must $\tau_f$ and $C_{c's}$ be?

10.22 A particular small-geometry BJT has $f_T$ of 10 GHz and $C_{c's} = 0.1$ pF when operated at $I_c = 1.0$ mA. What is $C_{c's}$ in this situation? Also, find $g_m$. For $\beta = 120$, find $r_s$ and $f_T$.

10.23 For a BJT whose unity-gain bandwidth is 2 GHz and $\beta_0 = 200$, at what frequency does the magnitude of $h_{fe}$ become 40? What is $f_T$?

*10.24 For a sufficiently high frequency, measurement of the complex input impedance of a BJT having (ac) grounded emitter and collector yields a real part approximating $r_s$. For what frequency, defined in terms of $\omega_s$, is such an estimate of $r_s$ good to within 10% under the condition that $r_s \leq r_{in}/10$?

10.25 Complete the table entries on the previous page for transistors (a) through (g), under the conditions indicated. Neglect $r_s$.

Section 10.3: High-Frequency Response of the CS and CE Amplifiers

10.26 In a particular common-source amplifier for which the midband voltage gain between gate and drain (i.e., $-g_m R_{ds}'$) is $-39$ V/V, the NMOS transistor has $C_{gs} = 1.0$ pF and $C_{ds} = 0.1$ pF. What input capacitance would you expect? For what range of signal-source resistances can you expect the 3-dB frequency to exceed 1 MHz? Neglect the effect of $R_C$.

D 10.27 In the circuit of Fig. P10.27, the voltage amplifier is ideal (i.e., it has an infinite input resistance and a zero output resistance).

(a) Use the Miller approach to find an expression for the input capacitance $C_{in}$ in terms of $A$ and $C$.

(b) Use the expression for $C_{in}$ to obtain the transfer function $V_o(s)/V_{in}(s)$.

(c) If $R_{sg} = 1$ k$\Omega$, and the gain $V_o/V_{sg}$ is to have a dc value of 40 dB and a 3-dB frequency of 100 kHz, find the values required for $A$ and $C$.

(d) Sketch a Bode plot for the gain and use it to determine the frequency at which its magnitude reduces to unity.

10.28 An ideal voltage amplifier having a voltage gain of $-1000$ V/V has a 0.2-pF capacitance connected between its output and input terminals. What is the input capacitance of the amplifier? If the amplifier is fed from a voltage source $V_{sg}$ having a resistance $R_{sg} = 1$ k$\Omega$, find the transfer function $V_o/V_{sg}$ as a function of the complex-frequency variable $s$ and hence the 3-dB frequency $f_T$ and the unity-gain frequency $f_T$.

D 10.29 A design is required for a CS amplifier for which the MOSFET is operated at $g_m = 5$ mA/V and has $C_{gs} = 5$ pF and $C_{gs} = 1$ pF. The amplifier is fed with a signal source having $R_{sg} = 1$ k$\Omega$, and $R_s$ is very large. What is the largest value of $R_s$ for which the upper 3-dB frequency is at least 6 MHz? What is the corresponding value of midband gain and gain–bandwidth product? If the specification on the upper 3-dB frequency can be relaxed by a factor of 3, that is, to 2 MHz, what can $A_M$ and $GB$ become?

10.30 Reconsider Example 10.3 for the situation in which the transistor is replaced by one whose width $W$ is half that of the original transistor while the bias current remains unchanged. Find modified values for all the device parameters along with $A_M$, $f_M$, and the gain–bandwidth product, $GB$. Contrast this with the original design by calculating the ratios of new value to old for $W$, $V_{GS}$, $g_m$, $C_{gs}$, $C_{ds}$, $C_{in}$, $A_M$, $f_M$, and $GB$.

D *10.31 In a CS amplifier, such as that in Fig. 10.3(a), the resistance of the source $R_{sg}$ is 100 k$\Omega$, amplifier

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