Laboratory 4: Biasing of Bipolar Transistors

Preliminary Exercises

In lecture, we studied the relative properties of different biasing circuits. Of particular interest was the sensitivity of these various circuits to transistor parameters. To demonstrate these properties, we will design three biasing circuits using typical transistor parameters of $\beta = 100$ and $V_{BE} = 0.7\text{V}$, then see how changes in β (to 50 and 300) affect their performance.

1. Design and Compare Three Bias Circuits

Design the following bias circuits using transistor parameters of $\beta = 100$ and $V_{BE} = 0.7\text{V}$ for npn transistors and $V_{EB} = 0.7\text{V}$ for pnp transistors. For all circuits, I_C and V_{CE} must meet the specified values within a tolerance of ±5%. For each circuit design, calculate I_C and V_{CE} from your chosen resistors and confirm that I_C and V_{CE} are within ±5% of the specifications. You should use only standard resistor values in your design, and each resistive element in the circuit should use only a single physical resistor (no series or parallel combinations). Standard resistor values have the following mantissas: 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, and 8.2.

(a) For the circuit in Fig. PL4.1(a), select the resistor values that establish an operating point of $I_C = 5\text{mA}$ and $V_{CE} = 6\text{V}$.

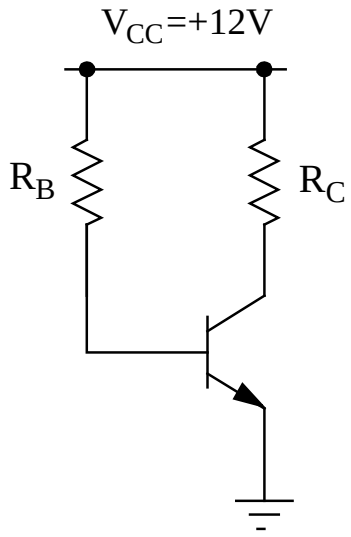

Figure PL4.1(a): Circuit 1

(b) For the circuit in Fig. PL4.1(b), select resistor values that establish an operating point of $V_{CE} = 5.5\text{V}$ and $I_C = 5\text{mA}$. V_E should be around 2.3V.

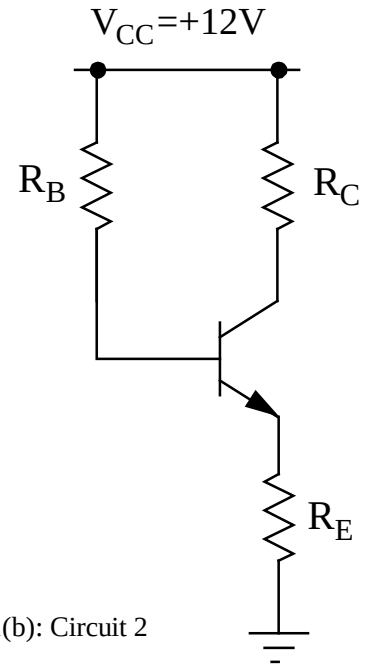

Figure PL4.1(b): Circuit 2

(c) Modify the circuit in part (b) as shown in Fig. PL4.1(c). This circuit should have the same operating point (V_{CE} and I_C). You should draw around 2.5 mA in the voltage divider formed by R_1 and R_2.

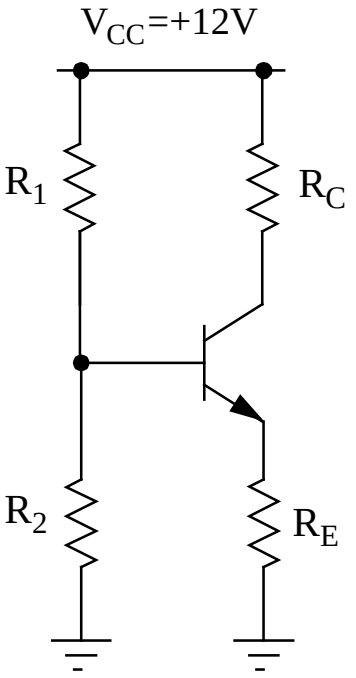

Figure PL4.1(c): Circuit 3

(d) Assume that we would like to bias pnp transistors to the same operating point as in the three circuits above. What simple circuit change (common to all three circuits) would be required?

2. Analysis of the Bias Circuits

(a) For each of the above circuits, compute the expected V_{CE} and I_C for $\beta = 50$, 100, and 300. Use these computations to fill in the tables on the *Results Sheet for Preliminary Exercises*. You can assume that $V_{BE} = 0.7\text{V}$ for npn transistors and $V_{EB} = 0.7\text{V}$ for pnp transistors. If $V_{CE} \leq V_{CE}(\text{sat}) \approx 0.2\text{V}$, also enter "saturated".

(b) Based on the above analysis, rank the circuits you designed in terms of sensitivity to β. The specifications are I_C and V_{CE}.

(c) Briefly explain why each circuit performed as it did in terms of β sensitivity.

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Results Sheet for Preliminary Exercises

NAME: _____ **LAB SECTION:** _____

1. Design of Three Biasing Circuits

(a) R_B = _____, R_C = _____

(b) R_B = _____, R_C = _____ , R_E = _____

(c) R_1 = _____, R_2 = _____

R_C = _____, R_E = _____

(d) What circuit modification would be required? Justify.

2. Analysis of the Bias Circuits

Values of I_C (npn/pnp)

CIRCUIT	β=50		β=100		β=300	
	npn	pnp	npn	pnp	npn	pnp
1						
2						
3						

Values of V_{CE} (npn/pnp)

CIRCUIT	β=50		β=100		β=300	
	npn	pnp	npn	pnp	npn	pnp
1						
2						
3						

(b) Rank the circuit "Least Sensitive" to "Most Sensitive"

Least _____

_____

Most _____

(c) Justify.