Lecture 14: MOSFETs II

- **Announcements**:
- HW#5 online and due Friday via Gradescope
- Lab#3 this week
  - ↳ Due week after next (since next week is the first midterm exam)
- Midterm 1: Friday, Oct. 5, from 5-6:30 p.m., in 277 Cory
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- Lecture Topics:
  - ↳ MOSFETs
    - — Linear Region
    - — Saturation Region
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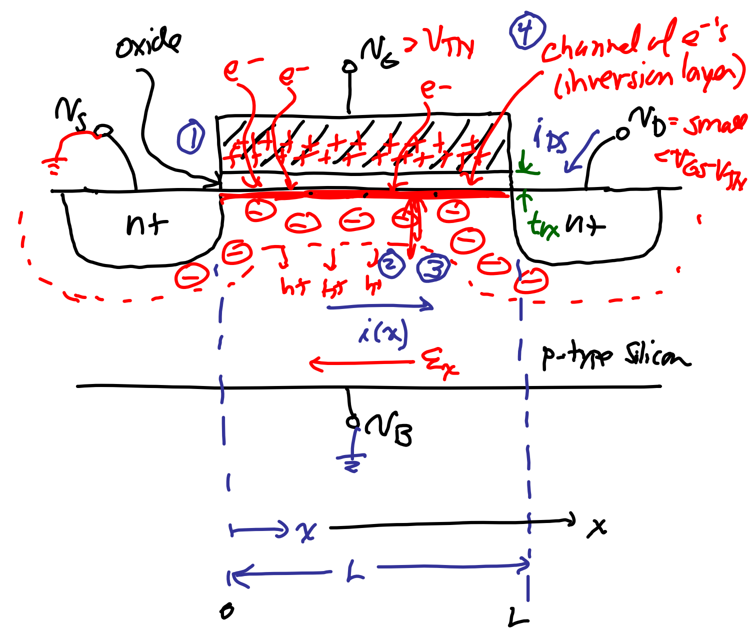
- **Last Time**:
- Started linear MOSFET operation
- Now, continue with this …

- As v_G rises:
  1. – More (+) charge amasses on the gate
  2. – The depletion region of fixed (-) charge grows to accommodate
  3. – Soon, however the depletion region becomes large enough that it becomes easier to obtain (-) charge (to match the gate's (+) charge) by taking it from the S/D regions!
  4. – **Result**: a channel of e-'s forms between the S&D n+ regions → inversion layer
  - – This happens when $v_{GS} > V_{TN}$

② Linear Region: (or Triode Region)

$(v_{GS} - V_{TN} \geq v_{DS} \geq 0) \rightarrow$ i.e., v_{DS} = small



- Channel of e-'s → mobile → silicon in this region now a conductor
- An E-field generated by v_{DS} gives rise to drift current flow

$\boxed{\text{Derive how much current } i_{DS} \text{ flows as a function voltages } v_{GS} \text{ \& } v_{DS}:}$

⇒ the e- drift current at any point in the channel:

$i(x) = Q'(x)\, v_x(x)$

$Q'(x)$: e- charge per unit length

$v_x(x)$: velocity of e-'s $= -\mu_n \mathcal{E}_x$

basically given by the charge on the gate-to-substrate capacitor:

$Q'(x) = -W C''_{ox}(v_{GS} - V_{TN} - v(x))$ ← $q = CV$

$-$: e-'s

$v(x)$: voltage in the channel at location x → at D, it's v_D; at S, it's $v_S = 0V$

$C''_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \triangleq$ oxide cap. per unit area

ϵ_{ox} = oxide permittivity $= 3.9\epsilon_0$

t_{ox} = oxide thickness [cm]

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$i(x) = \left[-W C''_{ox}(v_{GS} - V_{TN} - v(x))\right]\left[-\mu_n \mathcal{E}_x\right]$

$\left[\mathcal{E}_x = -\frac{dv(x)}{dx}\right]$

$i(x) = -\mu_n C''_{ox} W (v_{GS} - V_{TN} - v(x)) \frac{dv(x)}{dx}$

$i(x)\,dx = -\mu_n C''_{ox} W (v_{GS} - V_{TN} - v(x))\, dv(x)$

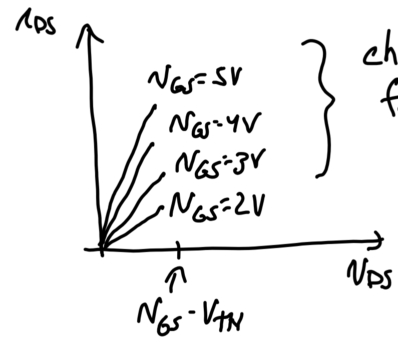
$\int_0^L i(x)\,dx = -\int_0^{v_{DS}} \mu_n C''_{ox} W (v_{GS} - V_{TN} - v(x))\, dv(x)$

But $|i(x)| = i_{DS}$ at all x; and $i(x) = -i_{DS}$

$i_{DS} L = \mu_n C''_{ox} W \left[(v_{GS} - V_{TN}) v_{DS} - \frac{v_{DS}^2}{2}\right]$

$\therefore \boxed{i_{DS} = \mu_n C''_{ox} \frac{W}{L}\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right) v_{DS}}$ (linear region) → small v_{DS}: $v_{DS} < v_{GS} - V_{TN}$

$\boxed{\text{Linear Region IV Characteristic}}$



characteristic curves look fairly linear for small v_{DS}

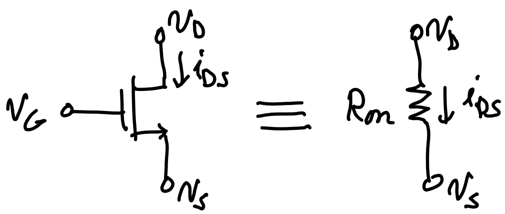
⇒ can define an equivalent small-signal (small v_{DS}) linear resistance for an MOS Xsistor in the linear region:

$$\frac{\partial i_{DS}}{\partial v_{DS}} = \mu_n C_{ox}'' \frac{W}{L}(v_{GS}-V_{TN}-v_{DS})$$

$$[v_{DS}=\text{small}] \Rightarrow \; \approx \mu_n C_{ox}'' \frac{W}{L}(v_{GS}-V_{TN})$$

$$\boxed{R_{on} = \left[\frac{\partial i_{DS}}{\partial v_{DS}}\right]^{-1} = \frac{1}{\mu_n C_{ox}'' \frac{W}{L}(v_{GS}-V_{TN})}}$$

↑ You'll need this for your next lab!



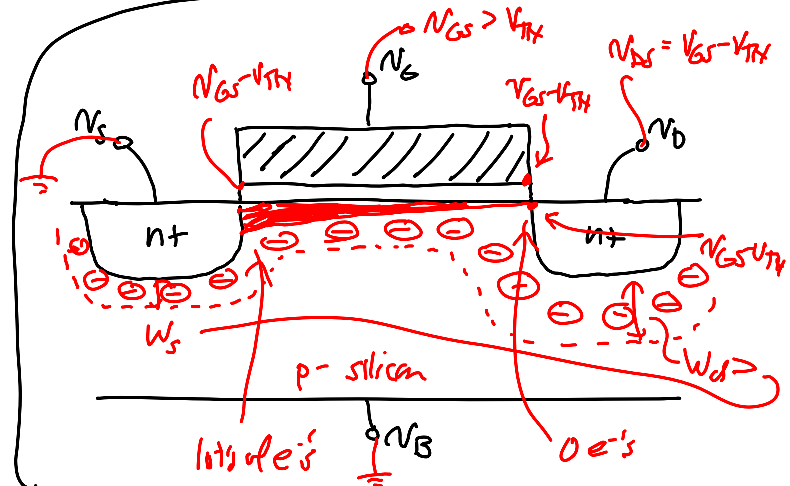
③ Saturation Region - ($v_{DS} \ge v_{GS}-V_{TN} \ge 0$)

As v_{DS}↑ → the voltage across the gate-to-substrate capacitor near the drain:

$(v_{GS}-V_{TN}-v(x)) \to 0$

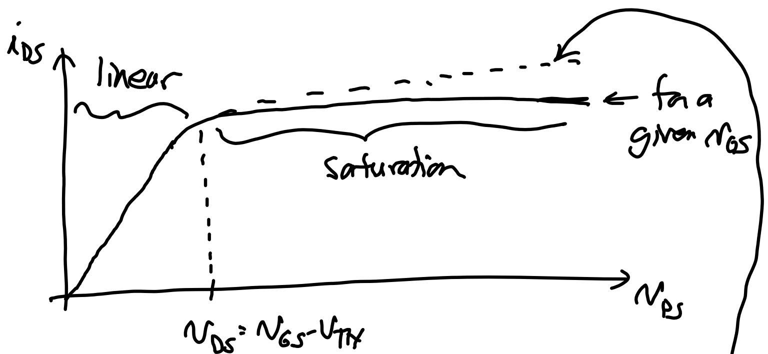
↑ @ the drain edge

At this point, i_{DS} has reached its ideal maximum! { ∴ the inversion charge @ the drain → 0!



Plug in $v_{GS}-V_{TN}-v_{DS}=0 \to v_{DS}=v_{GS}-V_{TN}$ into the i_{DS} equation:

$$i_{DS} = \frac{1}{2}\mu_n C_{ox}'' \frac{W}{L}(v_{GS}-V_{TN})^2 \quad \text{for } v_{DS}=v_{GS}-V_{TN}$$



⇒ as $v_{DS}\uparrow \rightarrow i_{DS} =$ const. ideally ... but due to 2nd order effects, i_{DS} actually still rises a bit

⇒ Reason: channel length modulation