

Lecture 15: MOSFETs III

- Announcements:
- HW#5 online and due Friday via Gradescope
- Lab#3 this week
 - ↳ Due week after next (since next week is the first midterm exam)
- Midterm 1: Friday, Oct. 5, from 5-6:30 p.m., in 277 Cory
- Lab Sections on different grading curves
 - ↳ Fairer for earlier lab sections
- Will be collecting names and student ID numbers for those who do not yet have access to the lab
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- Lecture Topics:
 - ↳ MOSFETs
 - Channel Length Modulation
 - Body Effect
 - ↳ Bipolar Junction Transistor (BJT)
 - Regions of Operation
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- Last Time:
- Started into channel length modulation
- Now, continue with this ...

③ Saturation Region - ($V_{DS} \geq V_{GS} - V_{TH} \geq 0$)

As $V_{DS} \uparrow \rightarrow$ the voltage across the gate-to-substrate

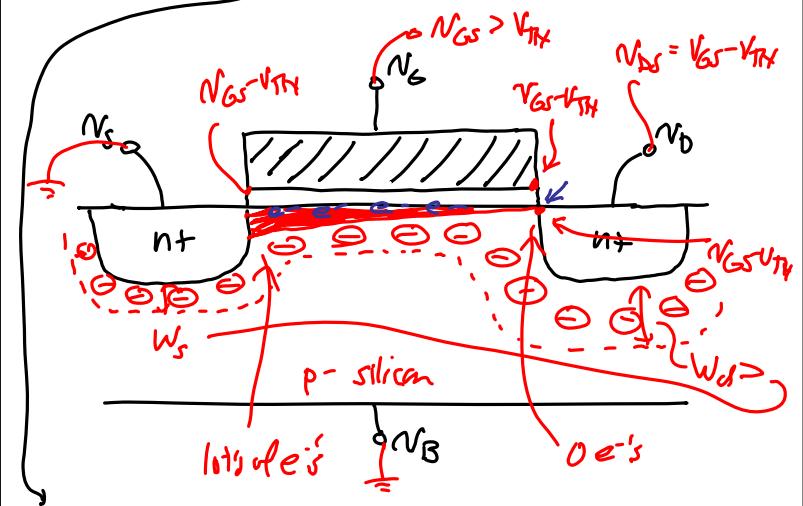
capacitance near the drain:

$$(V_{GS} - V_{TH} - V(x)) \rightarrow 0$$

↳ @ the drain edge

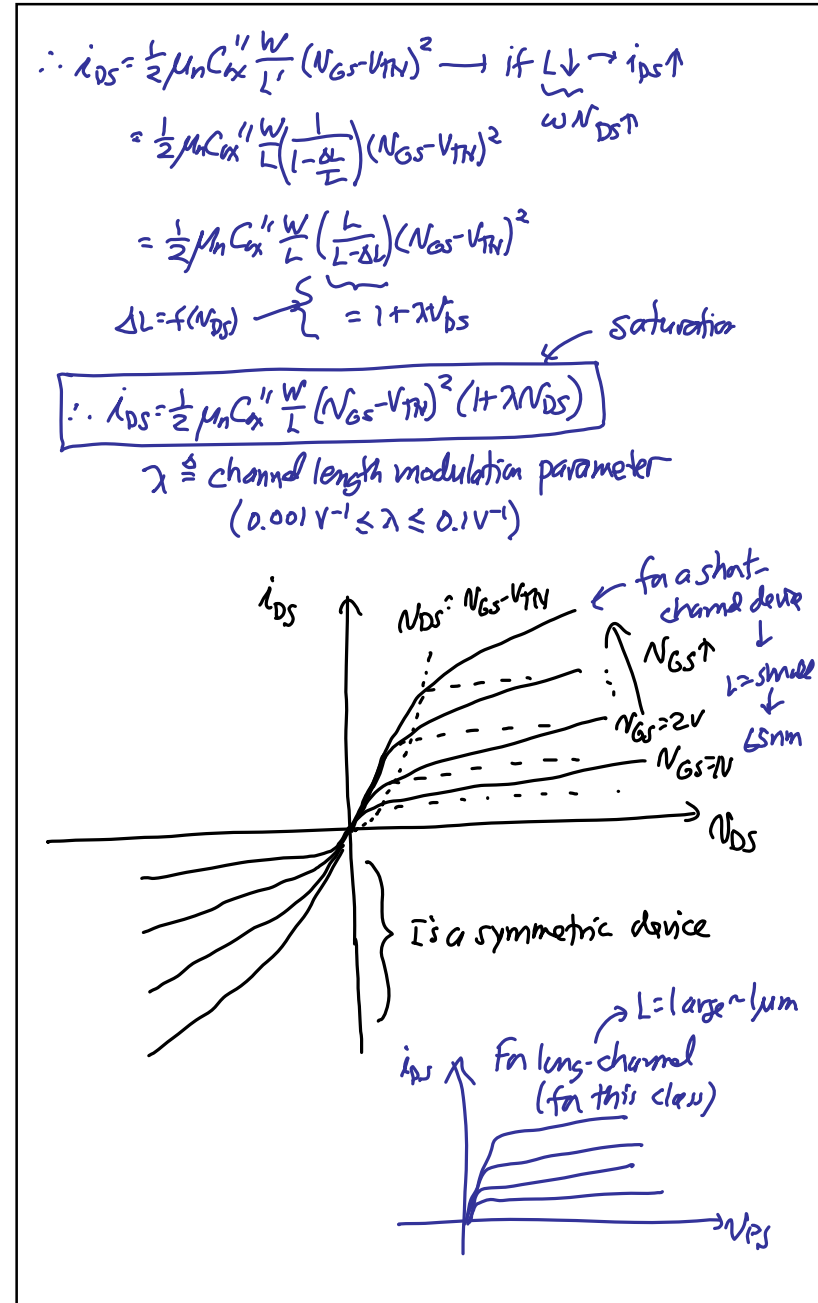
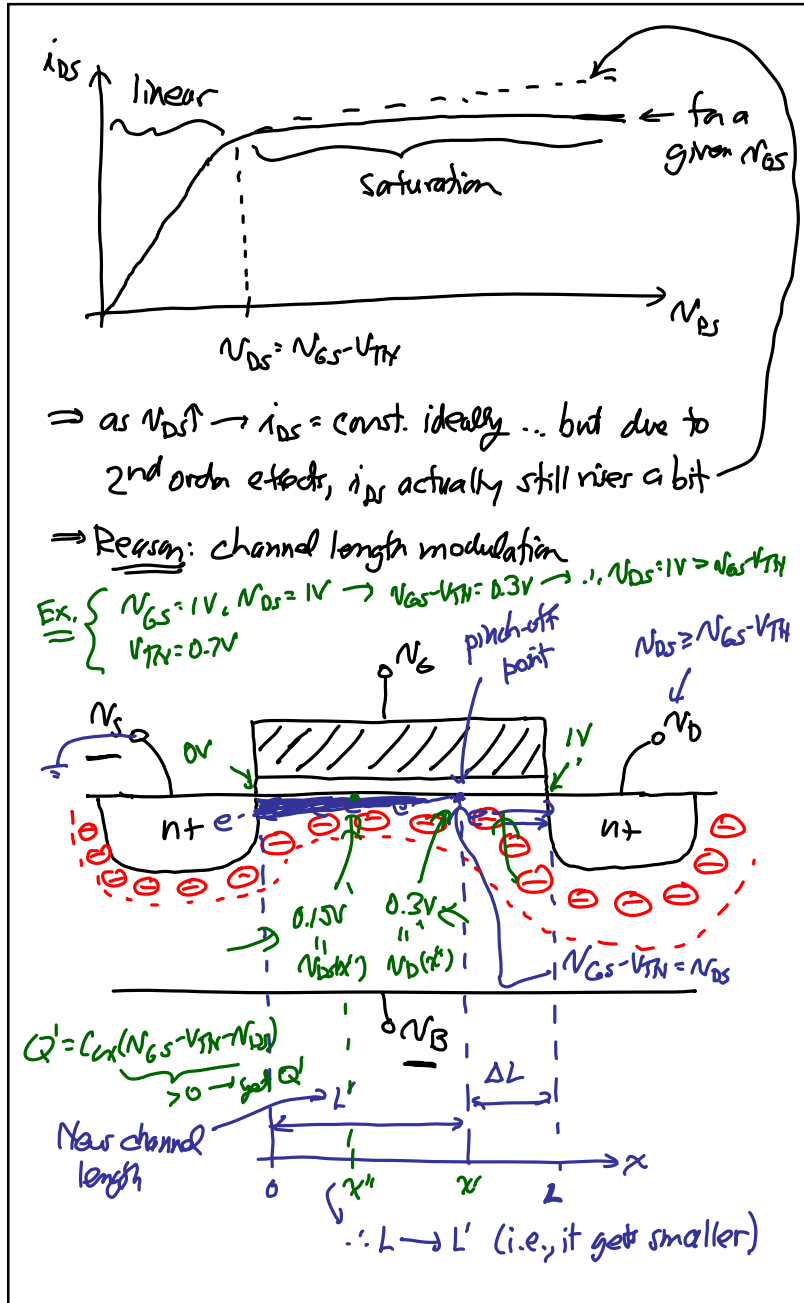
At this point, i_{DS} has reached its maximum! $\left\{ \begin{array}{l} \therefore \text{the inversion charge @} \\ \text{the drain} \rightarrow 0! \end{array} \right.$

↑
ideal



Plug in $V_{GS} - V_{TH} - V_{DS} = 0 \rightarrow V_{DS} = V_{GS} - V_{TH}$ into the i_{DS} equation:

$$i_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad \text{for } V_{DS} = V_{GS} - V_{TH}$$



Body Effect (Substrate Sensitivity)

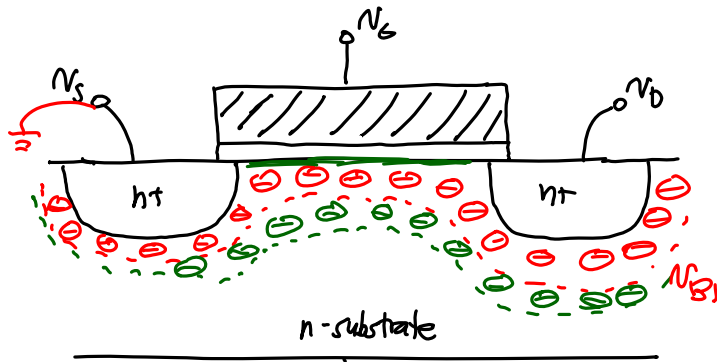
⇒ threshold voltage, V_{TN} , is a function of substrate bias voltage: V_{SB}

⇒ Reason: (simple version)

as $V_{SB} \uparrow \rightarrow$ max. channel depletion region gets larger (i.e., it can hold more charge)

need more V_{GS} to invert the channel

∴ $V_{TN} \uparrow$



Basically: $V_{SB} = 0V$

$$V_{TN} = V_{T0} + \gamma (\sqrt{N_{SB} + 2\phi_f} - \sqrt{2\phi_f})$$

where $V_{T0} \hat{=}$ value of V_{TN} for $V_{SB} = 0V$ [V]

$\gamma \hat{=}$ body effect parameter [V]

$2\phi_f \hat{=}$ surface potential parameter [V]

For a typical NMOS Transistor:

$-5V \leq V_{T0} \leq 5V \rightarrow$ but usually 0.7V
 $V_{T0} = (+) \rightarrow$ enhancement mode NMOS

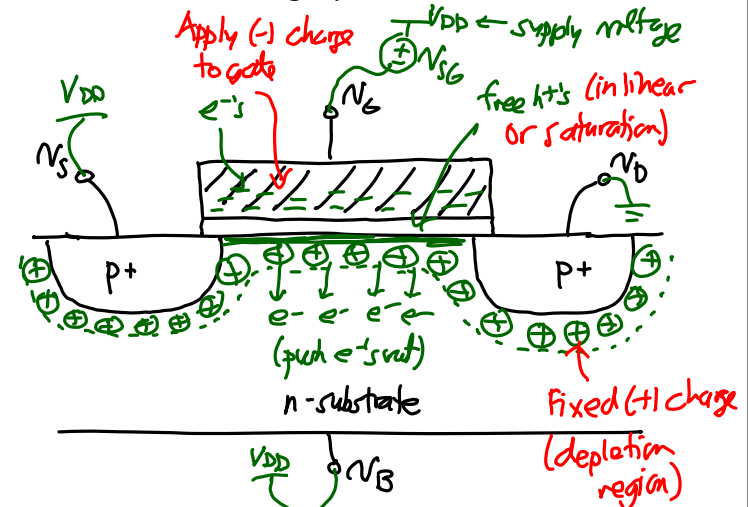
$V_{T0} = (-) \rightarrow$ depletion-mode NMOS
 (but out of the scope of this class)

$0 \leq \gamma \leq 3 \sqrt{V} \rightarrow$ typically, 0.5 \sqrt{V}

$0.3V \leq 2\phi_f \leq 1V \rightarrow$ for us, generally 0.6V

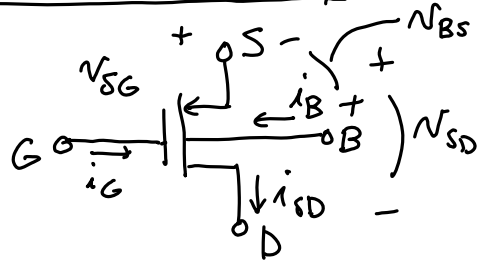
PMOS Transistors

- Basically, the reverse of NMOS transistors
- Physics basically the same, but the carriers are now h^+ and the voltage polarities reverse



$V_{TP} = (-)$ for an enhancement PMOS

PMOS Transistor Model Summary



① Cutoff Region: ($V_{SG} \leq -V_{TP}$)
 $i_{SD} = 0$

② Linear (or Triode) Region: ($V_{SG} + V_{TP} \geq V_{SD} \geq 0$)
$$i_{SD} = k_p \left(V_{SG} + V_{TP} - \frac{V_{SD}}{2} \right) V_{SD}$$
$$= \mu_p C_{ox}'' \frac{W}{L} \left(V_{SG} + V_{TP} - \frac{V_{SD}}{2} \right) V_{SD}$$

③ Saturation Region: ($V_{SD} \geq V_{SG} + V_{TP} \geq 0$)
$$i_{SD} = \frac{1}{2} \mu_p C_{ox}'' \frac{W}{L} (V_{SG} + V_{TP})^2 (1 + \lambda V_{SD})$$
$$= \frac{k_p}{2} (V_{SG} + V_{TP})^2 (1 + \lambda V_{SD})$$

where for all regions:

$$k_p = k_p' \frac{W}{L} = \mu_p C_{ox}'' \frac{W}{L}$$

$$i_G = 0 \text{ and } i_B = 0$$

$$V_{TP} = V_{T0} - \gamma \left(\sqrt{V_{BS} + 2\phi_f} - \sqrt{2\phi_f} \right)$$

$\mu_p \triangleq$ h^+ mobility in the channel

$C_{ox}'' \triangleq$ gate oxide per unit area

$V_{T0} \triangleq$ threshold voltage w/ $V_{SB} = 0V$

$\gamma \triangleq$ body effect parameter

$2\phi_f =$ built-in surface potential $\approx 0.6V$

