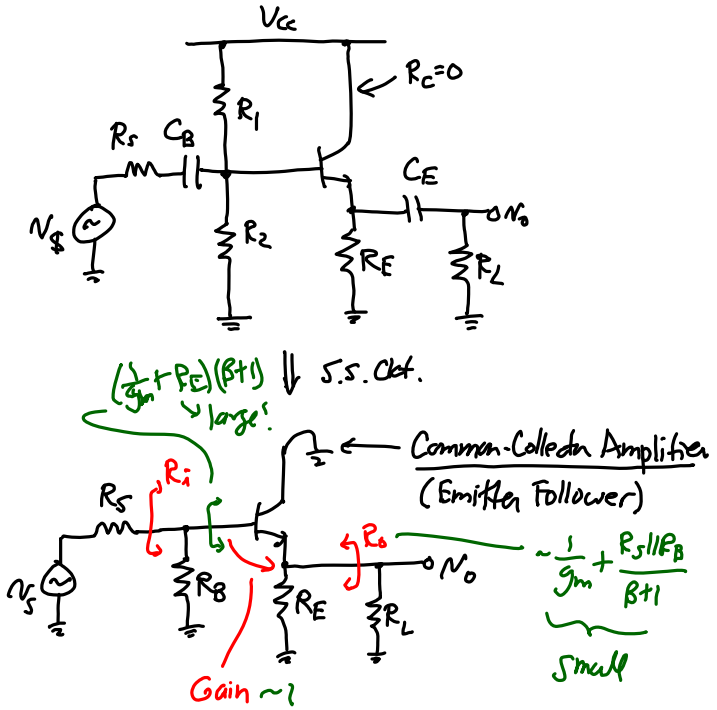
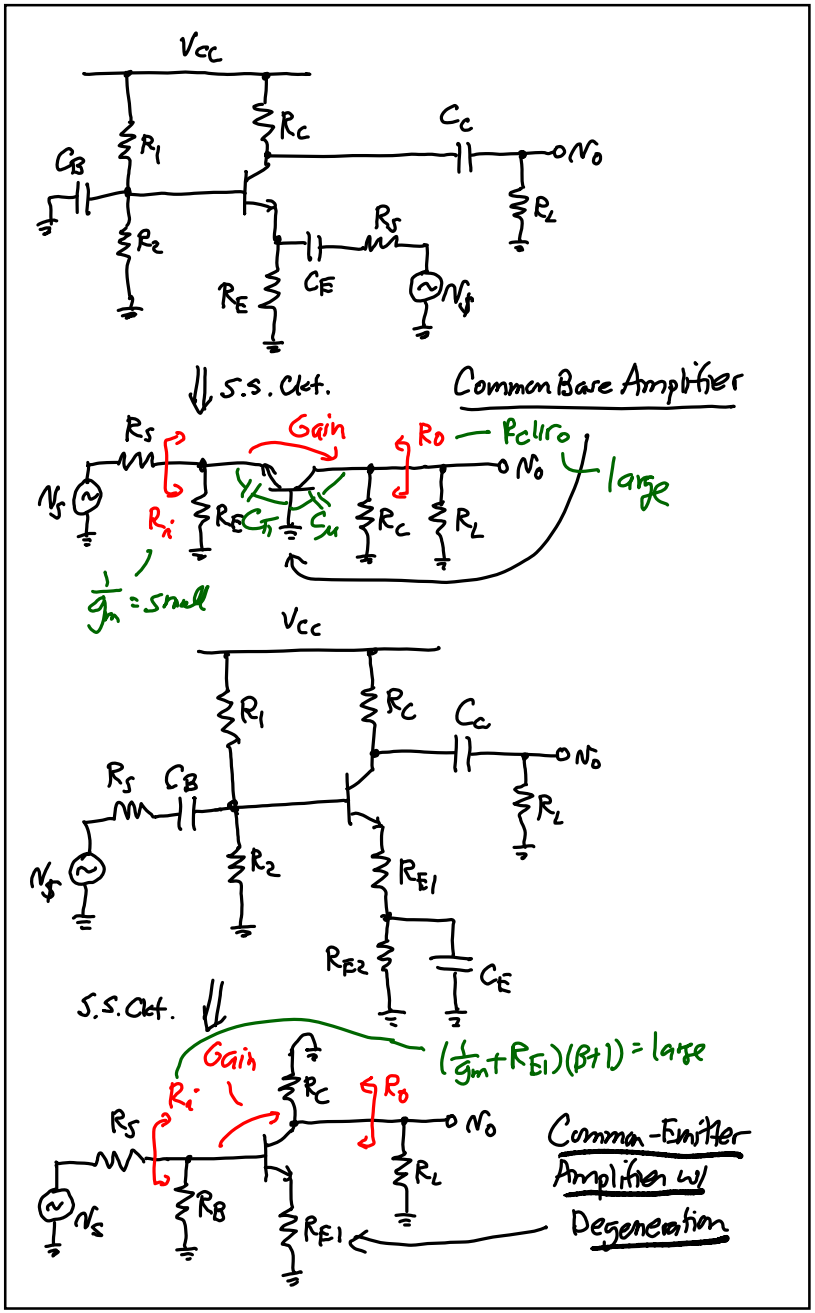
Lecture 34: Purposeful Design

- Announcements:
- HW#10 online and due Friday Nov. 16
- Midterm later today, Nov. 9, @ 5 p.m., in 277 Cory (just like last time)
  - We will have 2 hours for this exam
  - Midterm Info Sheet online
- Lab 6 online and due 5 p.m., Friday, Dec. 7
- Need to wait for Lecture 33 video
  - My computer hard drive crashed at the end of the last lecture
  - I did re-write the lecture, so you do have pdf online … but need to wait for the ETS video to appear on CalCentral
- No lecture next Monday
- Next lecture will be on Wednesday next week
- ----------
- Lecture Topics:
  - Purposeful Design
  - Cascode Amplifier
- ----------
- Last Time:
- Finished MOS inspection analysis
- Now consider design with a purpose
  - Very much needed for your Lab#6

Popular Amplifier Configurations → Building Blocks

- By merely altering the placements of input/output signals and bypass/coupling capacitors, one can realize many amplifier configurations
- Some of the most useful examples:





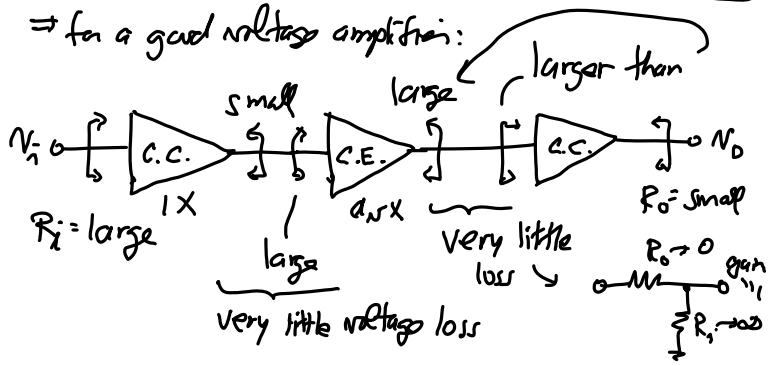
Multi-Stage Amplifier Design Guidelines

(for voltage amplifiers) (i→i amps, etc., would have different charts)

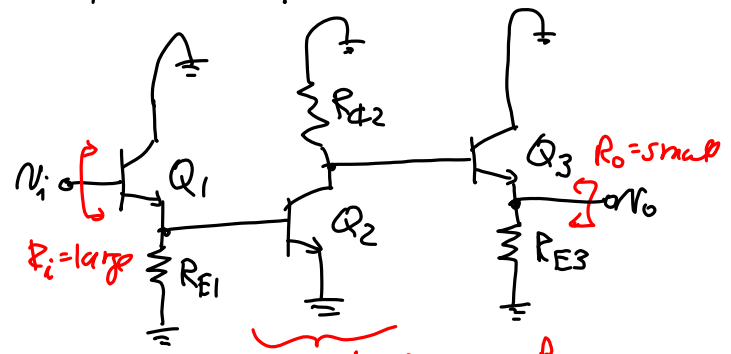
	Ideal Voltage Amp	C.E.	C.E. w/ R_E	C.C.	C.B.
R_i	∞	med. ✗	large ✓	large ✓	small ✗
R_o	0	large ✗	large ✗	small ✓	large ✗
a_v	∞	large ✓	med. ✗	small ✗	large ✓
f_H	∞	small ✗	med. ✗	large ✓	large ✓

To Get Better Performance → Cascade Amplifiers

⇒ for a good voltage amplifier:

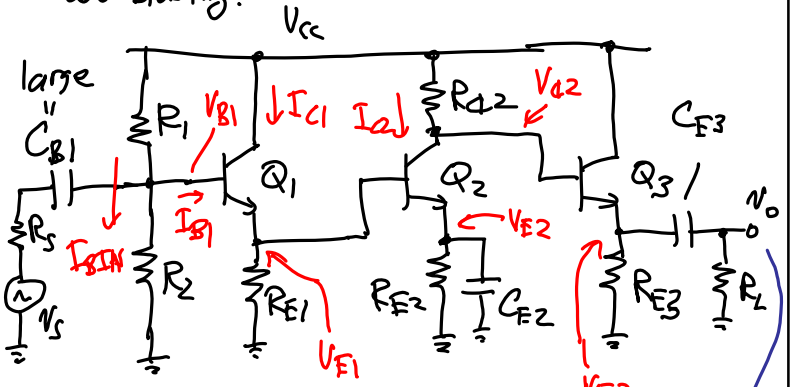


⇒ in the S.S. sense, we want:



good gain ~ $g_{m2}R_{C2}$

⇒ add biasing:



Biasing: for stability, $I_{BIAS} > 10 I_{B1}$

$V_{B1} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right)$ → $V_{E1} = V_{B1} - V_{BE(on)}$

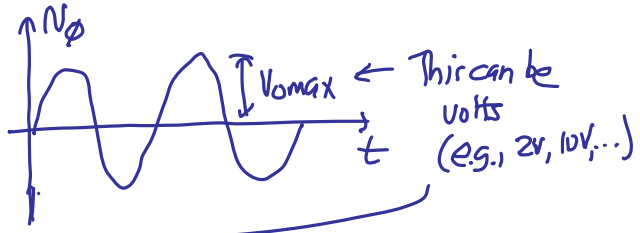
$I_{C1} \cong I_{E1} = \frac{V_{E1}}{R_{E1}}$

$V_{E2} = V_{E1} - V_{BE(on)}$
$= V_{B1} - 2V_{BE(on)}$

$I_{C2} \cong I_{E2} = \frac{V_{E2}}{R_{E2}}$ → $V_{C2} = V_{CC} - I_{C2}R_{C2}$

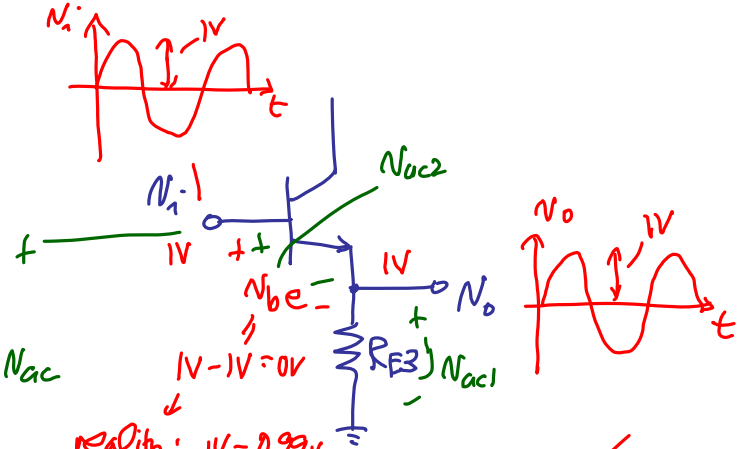
$V_{E3} = V_{C2} - V_{BE(on)}$ → $I_{C3} \cong I_{E3} = \frac{V_{E3}}{R_{E3}}$

* → Large Output Swing:



← This can be volts (e.g., 2V, 10V, ...)

↳ Does this violate our small-signal design criterion? → $v_{be} \ll V_T = 25mV$



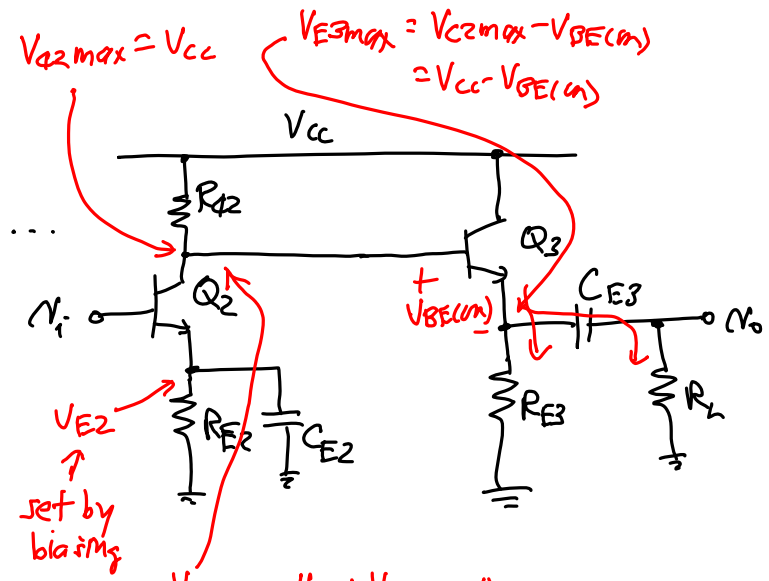
reality: 1V − 0.99V = 10 mV < 25mV ✓ satisfies small-signal

$v_{o1} \gg v_{o2}$

Emitter Follower Output Stage

⇒ What is the max voltage swing @ the output?

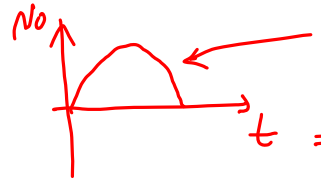
⇒ Need to think in both small & large signal domains



$V_{C2min} = V_{E2} + V_{CE2(sat)}$

$V_{E3min} = V_{E2} + V_{CE2(sat)} - V_{BE(on)}$ → on OV

Case: Max voltage

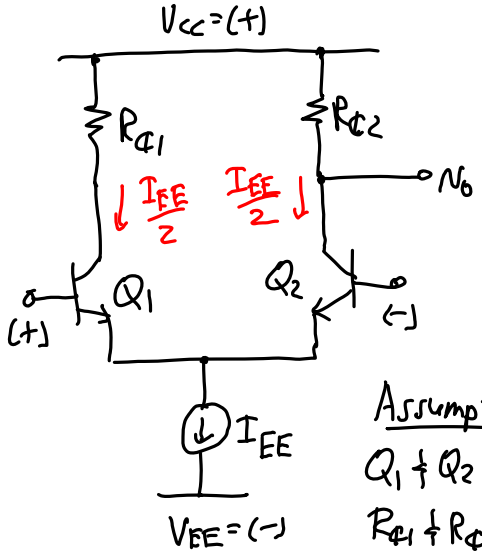


⇒ Q_3 sources enough current to push v_o up across $R_{E3} \| R_L$

⇒ max voltage limit determined by Q_2 stage

$$\therefore V_{omax} = \frac{V_{E3max} - V_{E3min}}{2}$$

Differential Pair → A Simple Op Amp



Assumptions:

Q_1 & Q_2 are identical

R_{C1} & R_{C2} identical