Lecture 36: Op Amp Design & Digital Circuits

- Announcements:
- HW#11 online soon and due during RRR week
- Lab 6 online and due 5 p.m., Friday, Dec. 7
- No ground class today, due to smoke
- This is a video recorded lecture
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- Lecture Topics:
  - MOS Op Amp Design
  - Review of Digital Electronics
  - Definitions
  - MOS Inverter w/ Resistive Load
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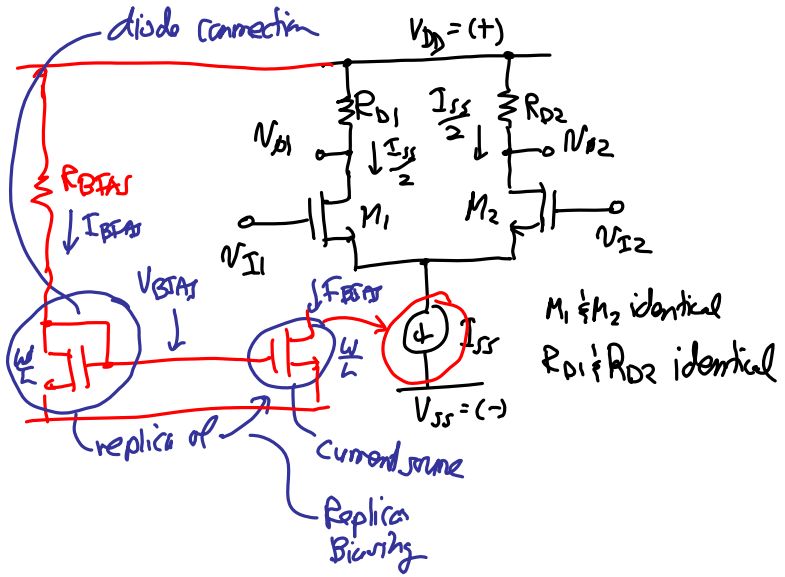
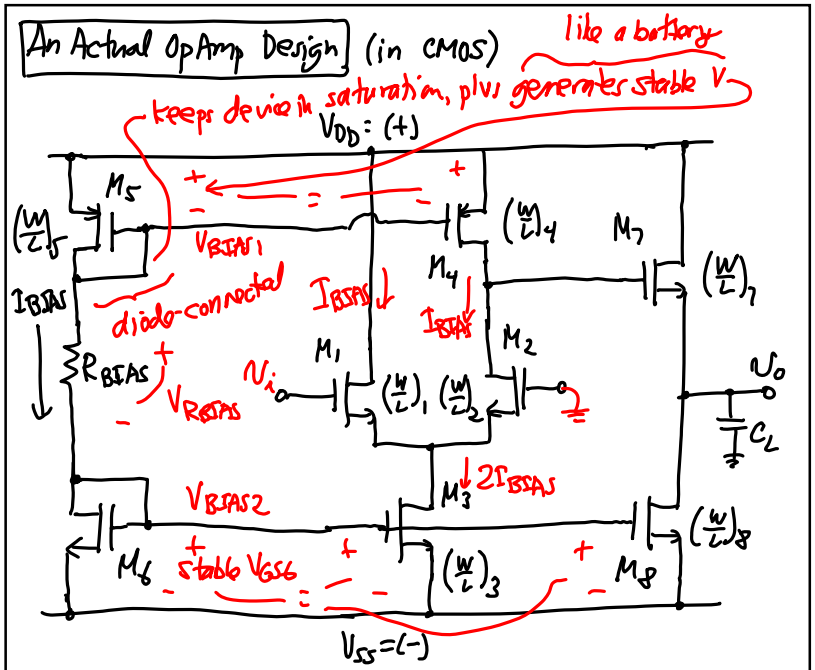
- Last Time:
- A first pass on differential pairs
  - Next pass will be in EE140 … but first …





$\left(\frac{W}{L}\right)_1=\left(\frac{W}{L}\right)_2$ → to eliminate V_{OS}

$\left(\frac{W}{L}\right)_4=\left(\frac{W}{L}\right)_5$ → for $I_{D4}=I_{D5}=I_{BIAS}$

$\left(\frac{W}{L}\right)_8=\left(\frac{W}{L}\right)_6$ → for $I_{D8}=I_{D7}=I_{D6}=I_{BIAS}$

$\left(\frac{W}{L}\right)_3=2\times\left(\frac{W}{L}\right)_6$ → for $I_{D3}=2I_{D6}=2I_{BIAS}$

To get I_{BIAS} (find R_{BIAS})

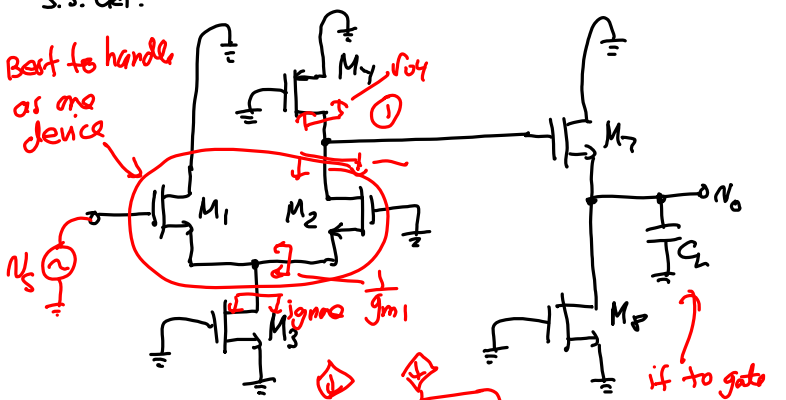
$$R_{BIAS}=\frac{V_{RBIAS}}{I_{BIAS}}=\frac{V_{DD}-|V_{GS5}|-V_{GS6}-V_{SS}}{I_{BIAS}}$$

$$I_{D5}=\tfrac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_5(|V_{GS5}|-|V_{tp}|)^2 \rightarrow |V_{GS5}|=|V_{tp}|+\sqrt{\frac{2I_{BIAS}}{\mu_p C_{ox}(W/L)_5}}$$

Similarly: $V_{GS6}=V_{tn}+\sqrt{\frac{2I_{BIAS}}{\mu_n C_{ox}(W/L)_6}}$

Gain ⇒ focus on the signal path only!

S.S. Ckt:



$$\frac{V_o}{V_s} = \frac{V_D}{V_s} \cdot \frac{V_o}{V_D}$$

V_s → $\frac{1}{g_{m1}}$, $\frac{1}{g_{m2}}$ → $i = \frac{V_s}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}}$

$$\frac{V_D}{V_s} = G_{mdiff} R_D = \underbrace{\frac{1}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}}}_{G_{mdiff}} \left(r_{o4} \| r_{o2}\left(1+\underbrace{\frac{g_{m2}}{g_{m1}}}_{2}\right)\right)$$

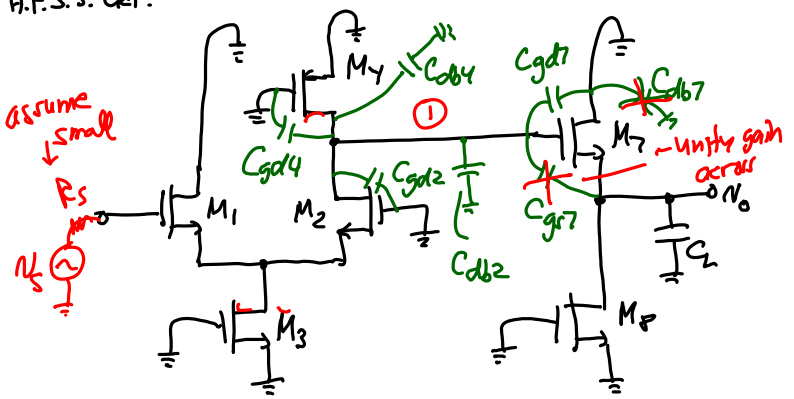
$$= \frac{1}{2} g_{m1}\left(r_{o4} \| (2r_{o2})\right)$$

$$\frac{V_o}{V_D} = \frac{g_{m7}}{g_{m7}+g_{mb7}} \approx 1$$

$$\therefore \frac{V_o}{V_s} = +\frac{1}{2} g_{m1}\left(r_{o4} \| (2r_{o2})\right)$$

High Freq. Cut-Off ⇒ focus on the highest impedance node → node ①

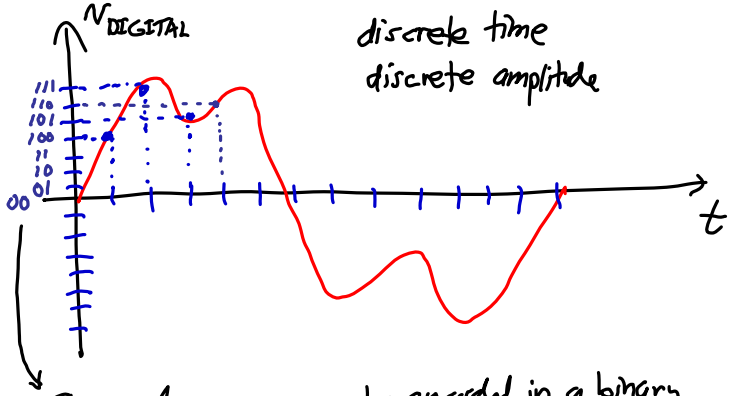
H.F.S.S. Ckt:



$$\omega_H = \frac{1}{\left(r_{o4} \| (2r_{o2})\right)\left\{C_{gd2}+C_{gd4}+C_{db4}+C_{db2}+C_{gd7}\right\}}$$

(this dominates the first pole)

- So far, our focus has been on analog amplifiers that process analog signals
- Earlier in the class, however, we looked at different signal types: analog, sampled-data, and digital
- Digital Signal:

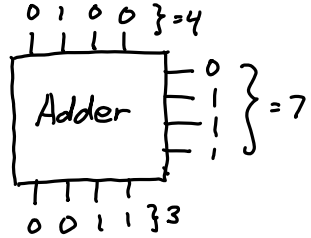


These values can now be encoded in a binary representation and processed via digital electronics

⇒ Problem: Lose information through quantization

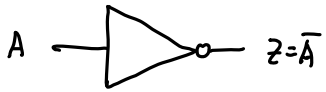
$$\text{Lost Info} \propto \frac{1}{\#\text{ of levels}}$$

- With enough levels, we can reduce quantization error to unnoticeable levels
- Then process via digital electronics, e.g., adder



- This class won't cover the design of this adder
- For now, suffice it to say that one way to design the adder is to put together a circuit of gates: inverters, NAND gates, NOR gates, etc.

Inverter

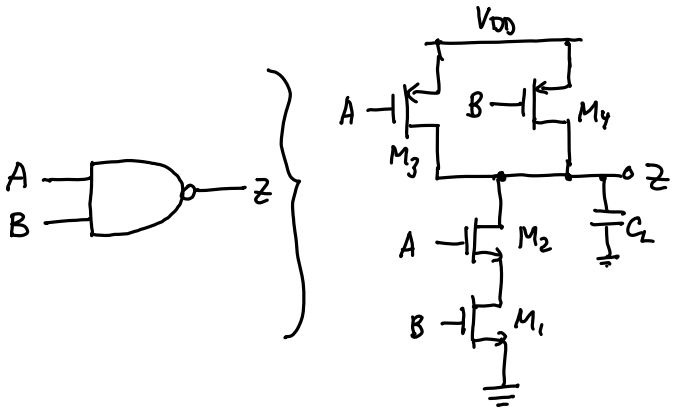


A	$Z = \bar{A}$
0	1
1	0

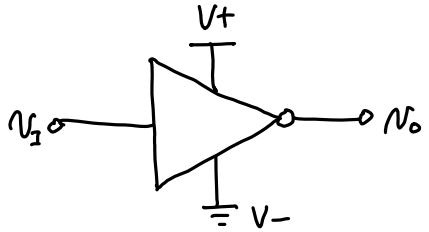
NAND

A	B	$Z = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

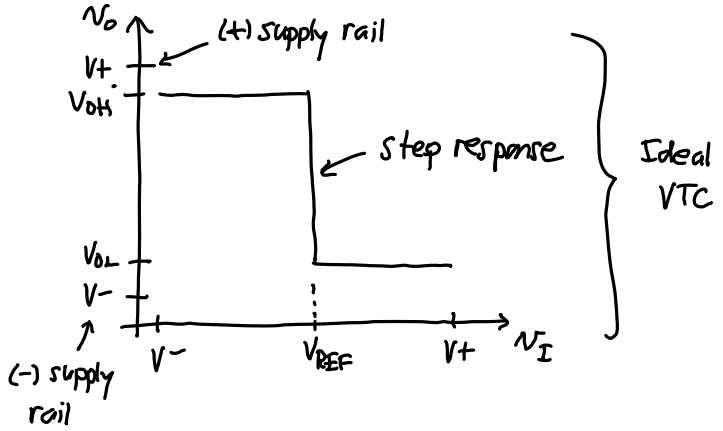
- Here, 0 → low voltage, 1 → high voltage
- If you have a NAND gate, you can make any digital function, including the adder above
- The NAND gate is a digital circuit that uses 4 transistors

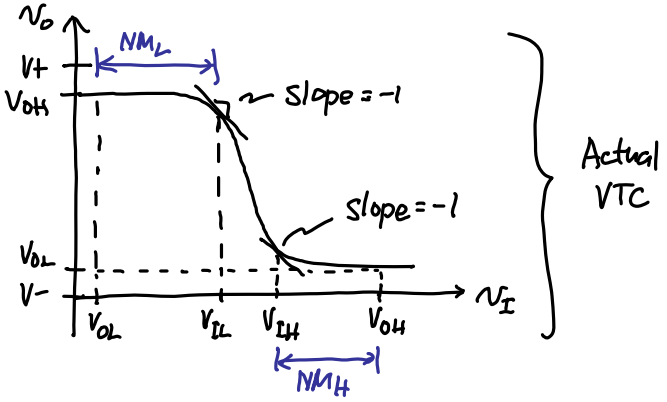


- The key to understanding this circuit starts with understanding a simpler circuit: the inverter



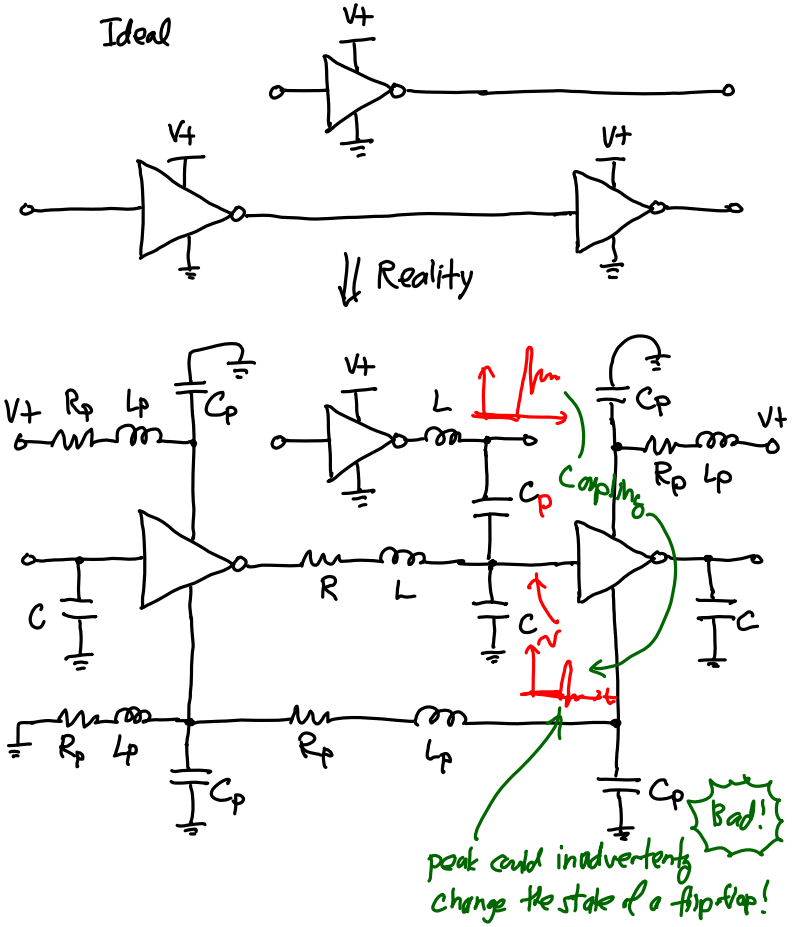
Voltage Transfer Characteristic (VTC)



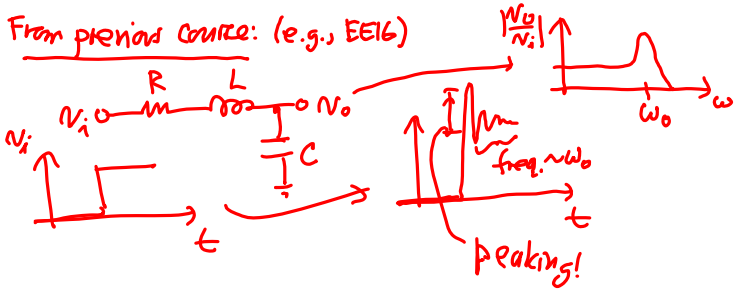


- V_{OL} = output low voltage (0)
- V_{OH} = output high voltage (1)
- V_{IL} = max. input voltage recognized as input low
- V_{IH} = min. input voltage recognized as input high
- $NM_L = V_{IL} - V_{OL}$ = noise margin low
- $NM_H = V_{OH} - V_{IH}$ = noise margin high

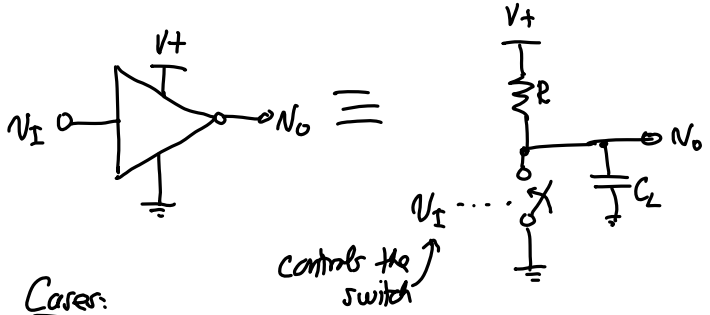
Why noise margins?



From previous course: (e.g., EE16)



Resistively-Loaded Inverter



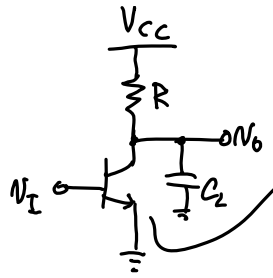
Cases:

① switch open: C_L charges to V+

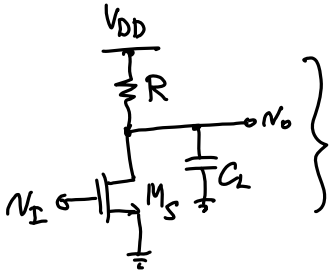
② switch closed: C_L discharges to ⏚

Transistor Inverter w/ Resistive Load

⇒ use Xsistor as a switching device → allowing it to handle large signals



bipolar not as good as MOS for digital
↳ reason: cost & power cons.

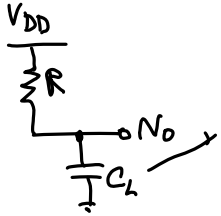


Find V_{OH} & V_{OL}.

Resistively-loaded MOS Inverter

V_{OH}: $V_I \le V_{IL}$ → say = 0V

⇒ M_S off

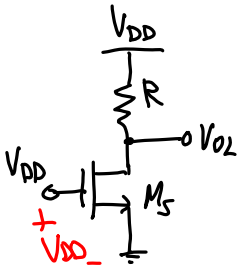


C_L charges to $V_O = V_{DD} = V_{OH}$

V_{OL}: $V_I \ge V_{IH}$ → say = V_{DD}

⇒ M_S on

⇒ in steady-state:



For M_S: $V_{GS} - V_{TNS} = V_{DD} - V_{TNS} > V_{OL}$

∴ M_S in linear!

$V_{OL} = V_{DD} - I_D R$

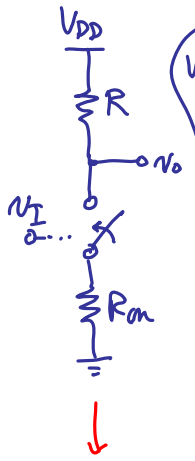
$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_S \left(V_{DD} - V_{TNS} - \frac{V_{OL}}{2}\right) V_{OL}$

$V_{OL} = V_{DD} - \mu_n C_{ox} \left(\frac{W}{L}\right)_S (V_{DD} - V_{TNS}) V_{OL} + \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_S}{2} V_{OL}^2$

⇒ solve quadratic for V_{OL}

⇒ or can get a less accurate (but still good) value...

⇒ ... by defining an on-resistance, R_{on}, for the switching device:

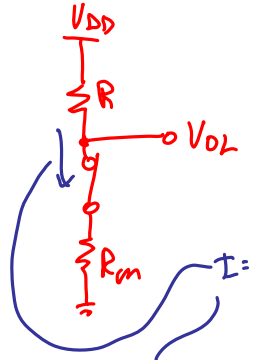


$$V_{OL} = V_{DD}\frac{R_{on}}{R+R_{on}} = V_{DD}\left(\frac{1}{1+\frac{R}{R_{on}}}\right)$$

$$R_{on} = \frac{v_{DS}}{i_D} = \frac{V_{OL}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left(V_{DD}-V_{TN}-\frac{V_{OL}}{2}\right)V_{OL}}$$

$$R_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left(V_{DD}-V_{TN}-\frac{V_{OL}}{2}\right)}$$

When $v_O = V_{OL}$



$$I = \frac{V_{DD}}{R+R_{on}}$$

⇒ in digital, any current is too much!

say $I = 1\mu A$ → okay for 100 transistors = $100\mu A$

↳ But for 1 billion → 1000A → way too much

↳ Thus, need lower power consumption → CMOS