

Lecture 37: CMOS Inverter

Announcements:

- HW#11 online and due during RRR week
- Lab 6 online and due 5 p.m., Friday, Dec. 7
- No ground class today, due to smoke
- This is a video recorded lecture

Lecture Topics: (over the next few days)

↳ **Static CMOS Inverter Behavior**

- V_{OL} and V_{OH}
- V_{IL} and V_{IH}

↳ **Dynamic CMOS Inverter Behavior**

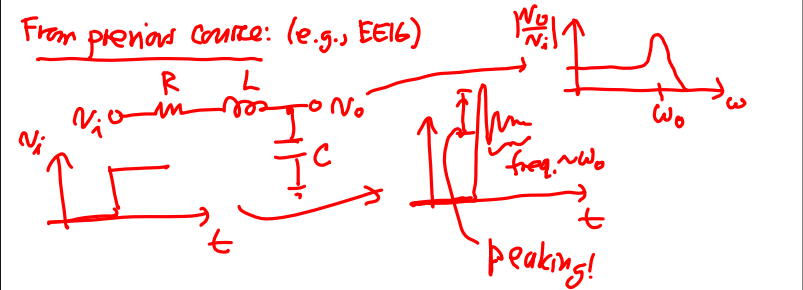
- Propagation Delay
- Capacitance

↳ **Astable Ring Oscillator**

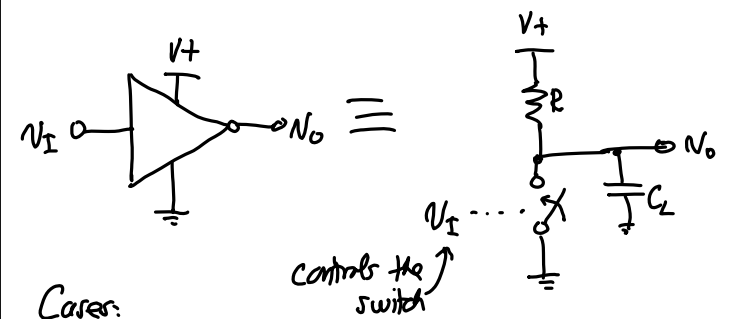
↳ **CMOS Inverter Propagation Delay**

Last Time:

- A first pass on differential pairs
 ↳ Next pass will be in EE140 ...
- Then started digital circuits



Resistively-Loaded Inverter

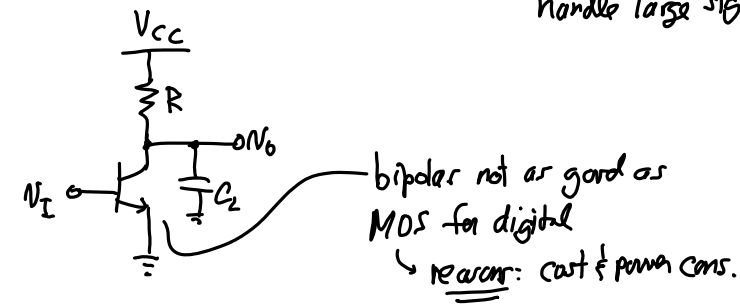


Cases:

- ① switch open: C_L charges to V_t
- ② switch closed: C_L discharges to \perp

Transistor Inverters w/ Resistive Load

= use transistor as a switching device → allowing it to handle large signals



Find V_{OH} & V_{OL} .

Resistively-Loaded MOS Inverter

V_{OH} : $V_I \leq V_{IL} \rightarrow \text{say } = 0V$
 $\Rightarrow M_S$ off

C_L charges to $N_O = V_{DD} = V_{OH}$

V_{OL} : $V_I \geq V_{IH} \rightarrow \text{say } = V_{DD}$
 $\Rightarrow M_S$ on
 \Rightarrow in steady-state:

For M_S : $V_{GS} - V_{TNS} = V_{DD} - V_{TNS} > V_{OL}$
 $\therefore M_S$ in linear!

$V_{OL} = V_{DD} - I_D R$
 $I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_S (V_{DD} - V_{TNS} - \frac{V_{OL}}{2}) V_{OL}$

$V_{OL} = V_{DD} - \mu_n C_{ox} \left(\frac{W}{L}\right)_S (V_{DD} - V_{TNS}) V_{OL} + \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_S V_{OL}^2}{2}$

\Rightarrow solve quadratic for V_{OL}
 \Rightarrow or can get a less accurate (but still good) value...

\Rightarrow ... by defining an on-resistance, R_{on} , for the switching device:

$V_{OL} = V_{DD} \frac{R_{OL}}{R + R_{on}} = V_{DD} \left(\frac{1}{1 + \frac{R}{R_{on}}} \right)$

$R_{on} = \frac{V_{DS}}{i_D} = \frac{V_{OL}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_S (V_{DD} - V_{TNS} - \frac{V_{OL}}{2})}$

$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_S (V_{DD} - V_{TNS} - \frac{V_{OL}}{2})}$

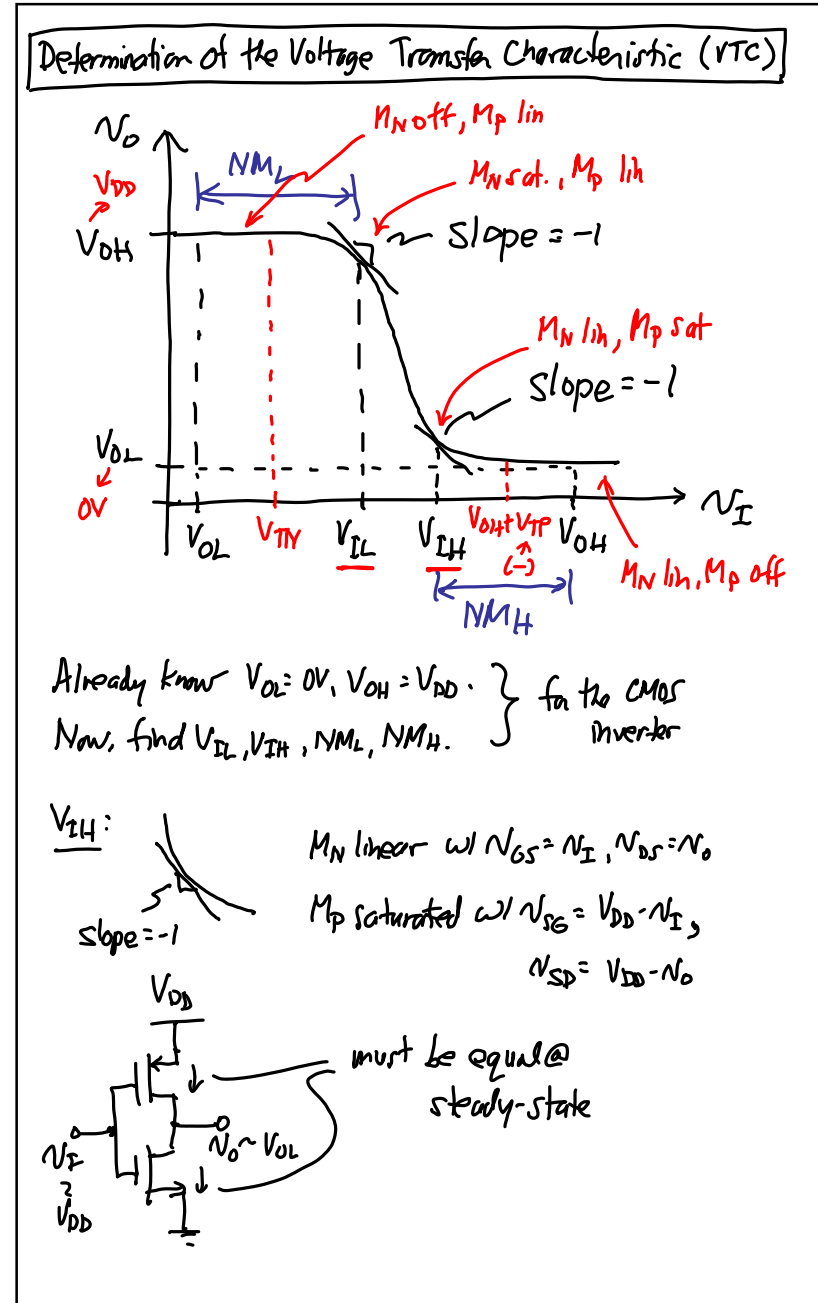
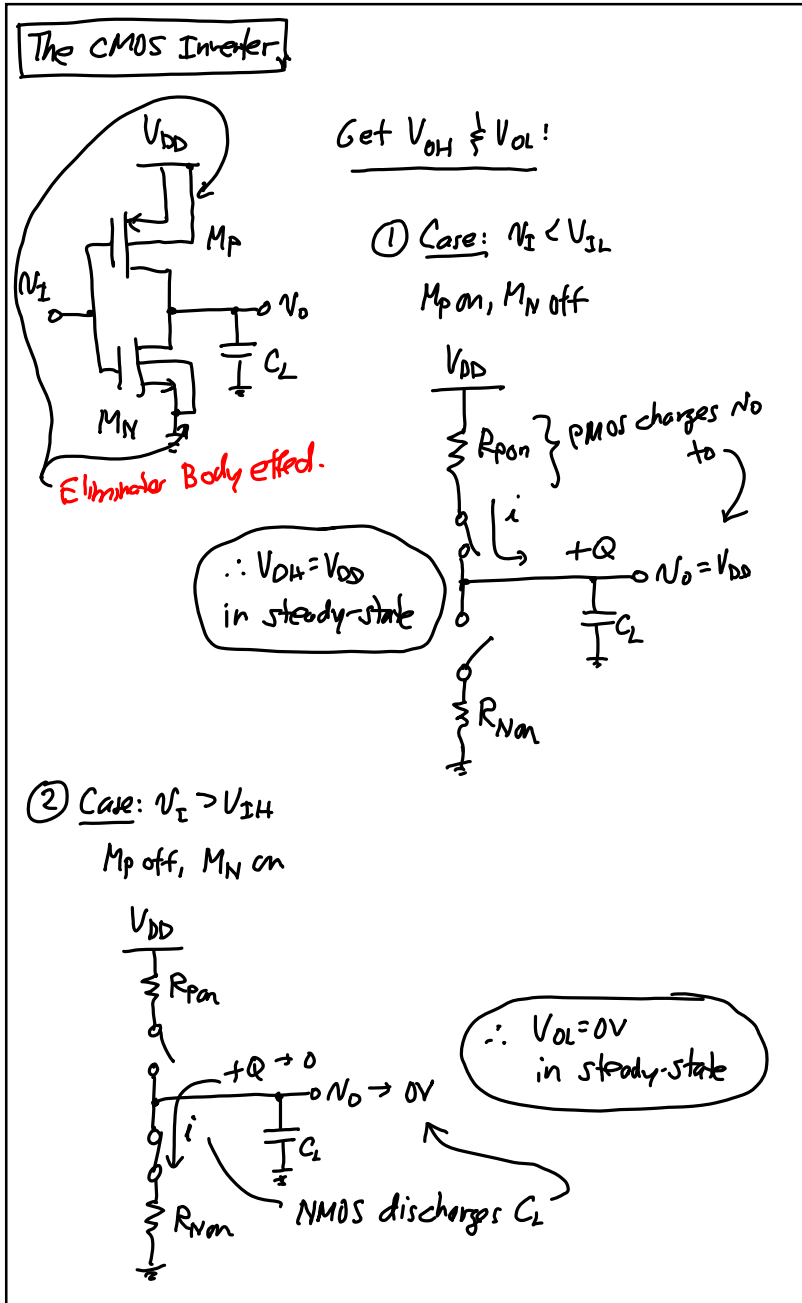
When $N_O = V_{OL}$

$I = \frac{V_{DD}}{R + R_{on}} \Rightarrow$ in digital, any current is too much!

Say $I = 1\mu A \rightarrow$ okay for 100 μ seconds = 100 μ ohms

But for 1 billion \rightarrow 1000A \rightarrow way too much

\rightarrow Thus, need lower power consumption \rightarrow CMOS



Thus: (equating drain currents)

$$i_{DSN}(lin) = i_{SDP}(sat.)$$

$$\underbrace{\mu_n C_{ox}}_{k_n} \left(\frac{W}{L}\right)_n (V_I - V_{TN} - \frac{V_o}{2}) N_o = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_p (V_{DD} - V_I + V_{TP})^2$$

$$[K_R = k_n/k_p] \Rightarrow K_R(2V_I - 2V_{TN} - V_o) N_o = (V_{DD} - V_I + V_{TP})^2$$

Solve for N_o : ... algebra ...

$$N_o = V_I - V_{TN} \pm \sqrt{(V_I - V_{TN})^2 - \frac{(V_{DD} - V_I + V_{TP})^2}{K_R}}$$

$\left[\frac{dN_o}{dV_I} = -1, N_I = V_{IH}\right] \Rightarrow$ Lots of math... using mathematics ...

$$V_{IH} = \frac{2K_R(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{1 + 3K_R}} - \frac{(V_{DD} - K_R V_{TN} + V_{TP})}{K_R - 1}$$

$$= \frac{2K_R(V_{DD} - V_{TN} - |V_{TP}|)}{(K_R - 1)\sqrt{1 + 3K_R}} - \frac{(V_{DD} - K_R V_{TN} - |V_{TP}|)}{K_R - 1}$$

one condensed form seen in literature

Problem: Not useful for the popular case

when $K_R = 1$, i.e., $k_n = k_p$

For $K_R = 1$, better to go back to the original constraining equations.

For $K_R = 1$:

$$(2N_I - 2V_{TN} - N_o) N_o = (V_{DD} - N_I + V_{TP})^2$$

$$(2N_I - 2V_{TN} - N_o) \frac{dN_o}{dN_I} + (2 - \frac{dN_o}{dN_I}) N_o = 2(V_{DD} - N_I + V_{TP}) \frac{dN_o}{dN_I}$$

$$\left[\frac{dN_o}{dN_I} = -1, N_I = V_{IH}\right] \Rightarrow$$

$$(2N_I - 2V_{TN} - N_o)(-1) + 3N_o = -2V_{DD} + 2N_I - 2V_{TP}$$

math

$$2N_o + V_{TN} + V_{TP} + V_{DD} = 2V_{IH}$$

$$V_{IH} = \frac{2N_o + V_{TN} + V_{TP} + V_{DD}}{2} \rightarrow N_o = \frac{1}{2}(2V_{IH} - V_{TN} - V_{TP} - V_{DD})$$

Lots of math...

$[N_I = V_{IH}]$

$$V_{IH} = \frac{5V_{DD} + 3V_{TN} + 5V_{TP}}{8}$$

math

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

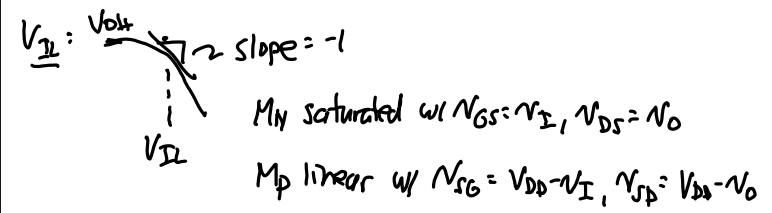
$$\therefore NM_H = \frac{3V_{DD} - 3V_{TN} - 5V_{TP}}{8}$$

Important Case:

- ⇒ NMOS & PMOS have identical strength
- ⇒ $V_{TN} = V_t, V_{TP} = -V_t$ (symmetrical V_t magnitudes)

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t), \quad NM_H = \frac{1}{8}(3V_{DD} + 2V_t)$$

- Remarks:
- $K_R = 1$ can be an important case when one wants the switching point to be at $V_{DD}/2$
- To get this case, one must size the PMOS bigger than the NMOS to give the former equal strength
- But if area is important (for cost reasons), then a designer will choose to use minimum-size devices, in which case the PMOS will not be as strong as the NMOS
 - ↳ The switch point will shift a bit from the midpoint of the supply
 - ↳ K_R not equal to 1



[Again, equate drain currents] ⇒

$$I_{SDP}(lin) = I_{DSN}(sat)$$

$$K_p(V_{DD} - V_{OL} + V_{TP})^2 - \frac{V_{DD} - V_{OL}}{2} = \frac{K_n}{2}(V_{OL} - V_{TN})^2$$

$\left[\frac{dV_{OL}}{dV_{IL}} = -1, V_{OL} = V_{IL} \right] \Rightarrow$ Again, lots of math...

$$V_{IL} = \frac{2\sqrt{K_R}(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{K_R + 3}} - \frac{(V_{DD} - K_R V_{TN} + V_{TP})}{K_R - 1}$$

$$= \frac{2\sqrt{K_R}(V_{DD} - V_{TN} - |V_{TP}|)}{(K_R - 1)\sqrt{K_R + 3}} - \frac{(V_{DD} - K_R V_{TN} - |V_{TP}|)}{K_R - 1}$$

↳ Again, not useful for $K_R = 1$.

Using a similar procedure to V_{IH} , can get

for $K_R = 1$:

$$V_{IL} = \frac{3V_{DD} + 5V_{TN} + 3V_{TP}}{8}, \quad NM_L = V_{IL}$$

... and for $K_R = 1$ & $V_{TN} = V_t, V_{TP} = -V_t$

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t) = NM_L$$

