Announcements:
- HW#11 online and due during RRR week
- Lab 6 online and due 5 p.m., Friday, Dec. 7
- We’re finally back from the smoke
- Z-scores at end of lecture today
- If fixed a couple of things in this
  First, the fact that Cdb goes from the drain to Vdd for the PMOS in an inverter
  Second, the tp equation, where tp = tp1 = tp2 = tp3, for the ring oscillator

Lecture Topics: (over the next few days)
- Static CMOS Inverter Behavior
  - $V_{OL}$ and $V_{OH}$
  - $V_{IL}$ and $V_{IH}$
- Dynamic CMOS Inverter Behavior
  - Propagation Delay
  - Capacitance
- Astable Ring Oscillator
- CMOS Inverter Propagation Delay

Last Time:
- Ended up defining propagation delay
Remarks
Propagation delay is the delay experienced by a signal passing through a gate as measured between the 50\% transition points between input and output waveforms.
In general, a gate displays different response times for rising and falling input waveforms.
Thus, define:
- \( t_{\text{PLH}} \): response time of a gate making a low→high output transition
- \( t_{\text{PHL}} \): response time of a gate making a high→low output transition
Propagation delay then defined as the average of \( t_{\text{PLH}} \) and \( t_{\text{PHL}} \).

What causes switching delay?
- Finite current transistor current drive (i.e., finite on resistance \( R_{\text{on}} \))
- Output node capacitance

\[
C_{\text{d}} = \frac{C_{gds}}{\sqrt{f(V_{gs})}} = \frac{C_{gds}}{(1 + \frac{V_{gs}}{\Phi})}
\]
EE 105: Microelectronic Devices & Circuits
Lecture 38w: Propagation Delay

Propagation Delay in CMOS Inverter

\[ T = \frac{1}{2} T_{PD} + T_{PHL} + T_{PHO} \]

\[ t_{PHL} + t_{PHO} \text{ gives a value for the delay across this two-stage inverter chain} \]

\[ \frac{1}{2} T = t_{PD} + t_{PH} + t_{PH} \]

\[ t_{PH} = t_{PH} + t_{PH} = t_{PH} \]

\[ \Rightarrow \frac{1}{2} T = N \tau_{p} \rightarrow T = 2 N \tau_{p} = \frac{1}{2 \tau_{p}} \]

\[ \text{oscillation freq.} \]

\[ \text{no. of inverters} \]