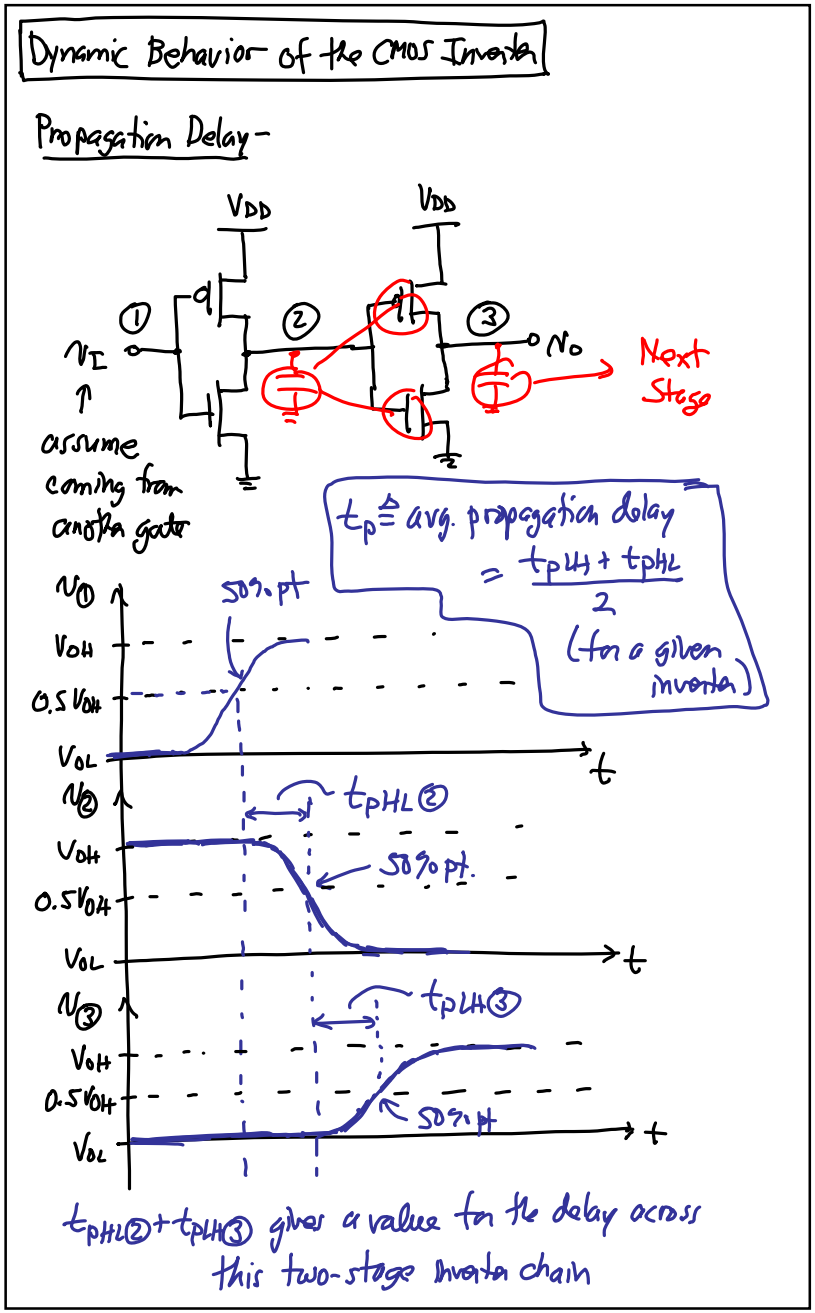
EE 105: Microelectronic Devices & Circuits
Lecture 38w: Propagation Delay

Lecture 38: Propagation Delay I

- Announcements:
- HW#11 online and due during RRR week
- Lab 6 online and due 5 p.m., Friday, Dec. 7
- We're finally back from the smoke
- Z-scores at end of lecture today
- If fixed a couple of things in this
  - First, the fact that Cdb goes from the drain to Vdd for the PMOS in an inverter
  - Second, the tp equation, where tp = tp1 = tp2 = tp3, for the ring oscillator
- ----------
- Lecture Topics: (over the next few days)
  - Static CMOS Inverter Behavior
    - V_{OL} and V_{OH}
    - V_{IL} and V_{IH}
  - Dynamic CMOS Inverter Behavior
    - Propagation Delay
    - Capacitance
  - Astable Ring Oscillator
  - CMOS Inverter Propagation Delay
- ----------
- Last Time:
- Ended up defining propagation delay



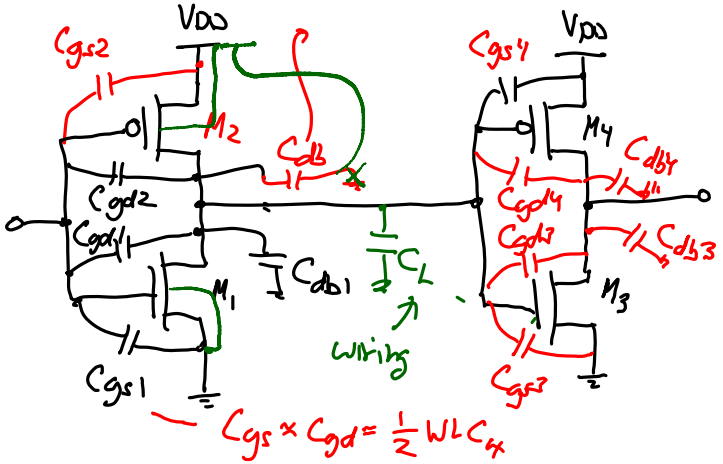
Copyright © 2018 Regents of the University of California

EE 105: Microelectronic Devices & Circuits
Lecture 38w: Propagation Delay

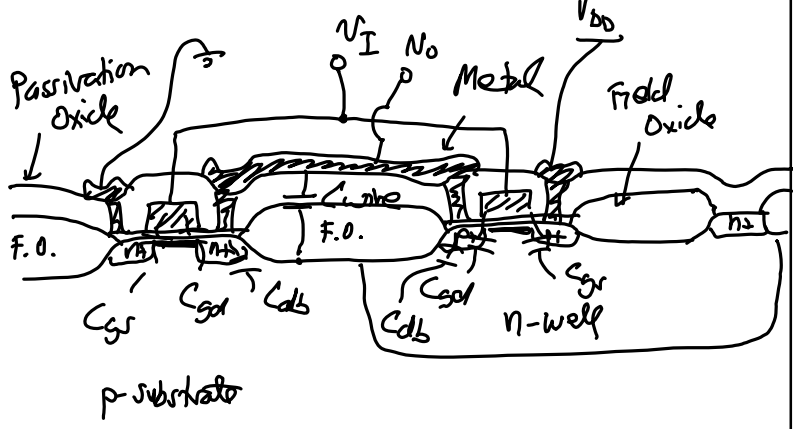
- Remarks
- Propagation delay is the delay experienced by a signal passing through a gate as measured between the 50% transition points between input and output waveforms
- In general, a gate displays different response times for rising and falling input waveforms
- Thus, define:
  - t_{pLH}: response time of a gate making a low→high output transition
  - t_{pHL}: response time of a gate making a high→low output transition
- Propogation delay then defined as the average of t_{pLH} and t_{pHL}
- What causes switching delay?
  - Finite current transistor current drive (i.e., finite on resistance R_{on}
  - Output node capacitance

Capacitance

$$C_{db} = \frac{C_{db0}}{\sqrt{f(V_{DD})}} \cdot \left(\frac{C_{db0}}{1 + \frac{V_{DD}}{\phi_j}}\right)^m$$



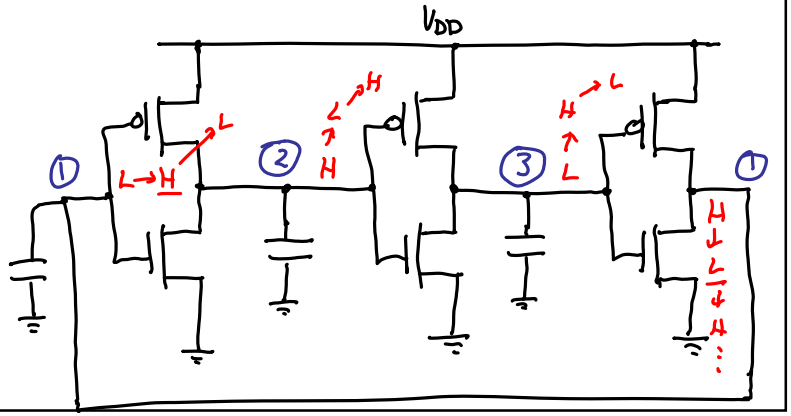
Actual CMOS (old) (an inverter)



⇒ take EE143 to learn MORE!!!

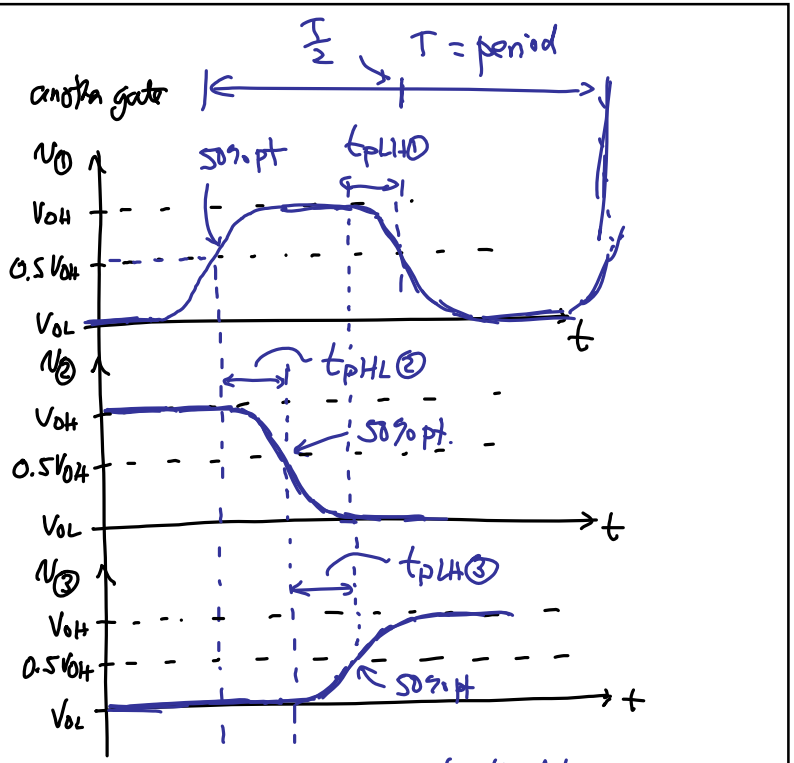
Astable Ring Oscillator

⇒ what is an oscillator? → a device that puts out a stable frequency!



Copyright © 2018 Regents of the University of California

EE 105: Microelectronic Devices & Circuits
Lecture 38w: Propagation Delay



$t_{pHL②} + t_{pLH③}$ gives a value for the delay across this two-stage inverter chain

$\frac{1}{2}T = t_{p①} + t_{p②} + t_{p③}$

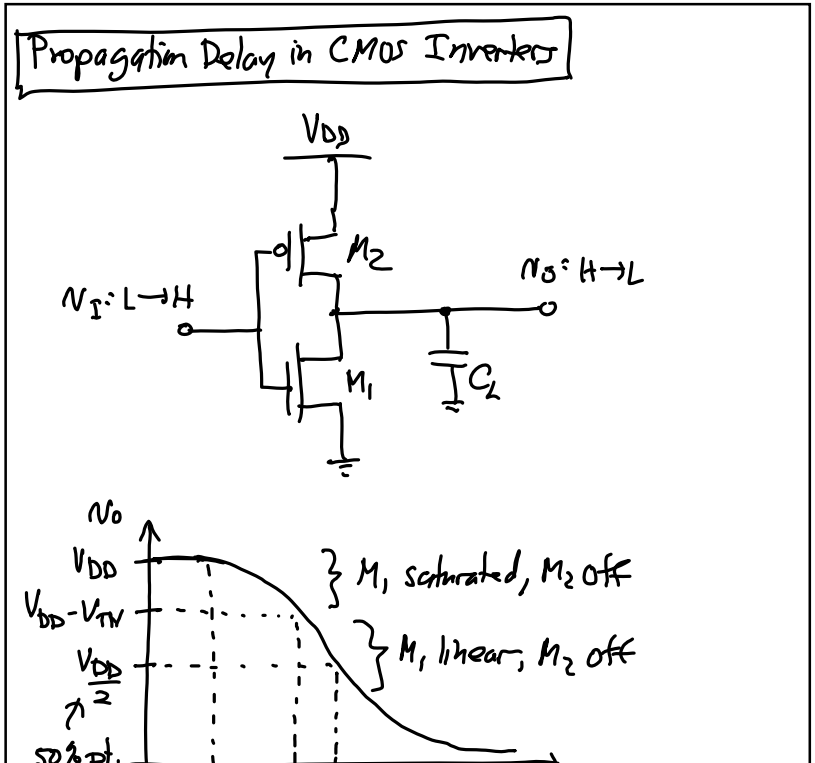
[Identical & symmetric inverters] $\Rightarrow$

$t_p = t_{p①} = t_{p②} = t_{p③}$

$\Rightarrow \frac{1}{2}T = Nt_p \rightarrow T = 2Nt_p \Rightarrow f_o = \frac{1}{2Nt_p}$

(f_o: oscillation freq.)

(N: no. of inverters)



Copyright © 2018 Regents of the University of California