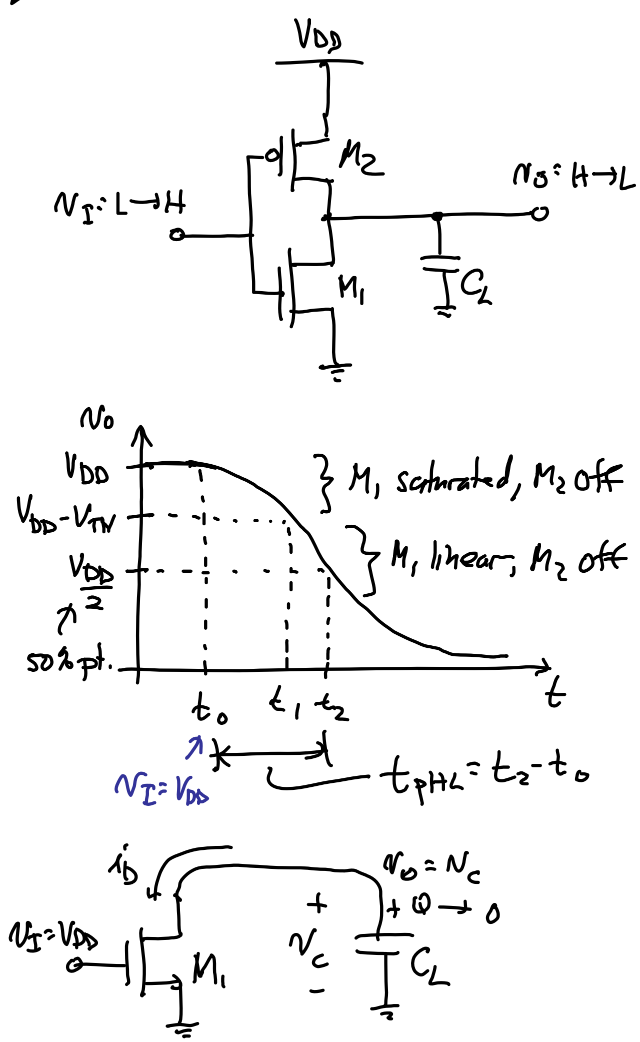
EE 105: Microelectronic Devices & Circuits
Lecture 40w: Complex Gates

Lecture 40: Complex Gates

- **Announcements**:
- Last lecture!
- HW#11 online and due during RRR week
- Lab 6 online and due 5 p.m., Friday, Dec. 7
- Labs will run as usual next week
- We will keep all normal office hours during RRR Week and Finals Week up through the Wednesday before the Final Exam
- There will be extra office hours during Finals Week, as explained in the Final Exam Info Sheet
- ------------------------------------
- Lecture Topics: (over the next few days)
  - Complex CMOS Gates
  - Final Exam Info Sheet
- ------------------------------------
- **Last Time**:
- Finished the expression for CMOS inverter t_{pHL} propagation delay
- Now summarize this …

Propagation Delay in CMOS Inverters



Case: $v_O \geq V_{DD}-V_{TN} \rightarrow M_1$ saturated

$$i_{D(sat)} = \frac{K_N}{2}(v_{GS}-V_{TN})^2 = -C_L\frac{dv_C}{dt}$$

$$dt = \frac{-2C_L\,dv_C}{K_N(v_{GS}-V_{TN})^2} = \frac{-2C_L\,dv_C}{K_N(V_{DD}-V_{TN})^2}$$

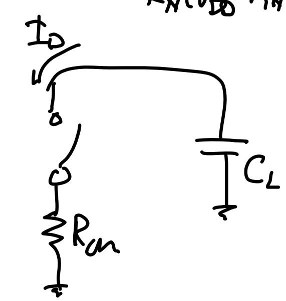
$$[v_{GS}=V_{OH}=V_{DD}=v_I]$$

$$\int_{t_0}^{t_1} dt = \int_{V_{DD}}^{V_{DD}-V_{TN}} -\frac{2C_L}{K_N(V_{DD}-V_{TN})^2}$$

$$(t_1-t_0) = -\frac{2C_L}{K_N(V_{DD}-V_{TN})^2}(\cancel{V_{DD}}-V_{TN}-\cancel{V_{DD}})$$

$$\boxed{(t_1-t_0) = \frac{2C_L}{K_N(V_{DD}-V_{TN})}\frac{V_{TN}}{V_{DD}-V_{TN}} = 2C_L R_{on}\frac{V_{TN}}{V_{DD}-V_{TN}}}$$

effective "on resistance" of the Xsistor $\rightarrow R_{on} = \frac{1}{K_N(V_{DD}-V_{TN})}$



Case: $v_O < V_{DD}-V_{TN} \rightarrow M_1$ linear

$$i_{D(lin)} = -C_L\frac{dv_C}{dt}$$

$$K_N\left(v_{GS}-V_{TN}-\frac{v_{DS}}{2}\right)v_{DS} = -C_L\frac{dv_C}{dt}$$

$$[v_{DS}=v_C,\ v_{GS}=V_{DD}] \Rightarrow \left\{K_N\left(V_{DD}-V_{TN}-\frac{v_C}{2}\right)v_C = -C_L\frac{dv_C}{dt}\right\}\times 2$$

$$\int_{t_1}^{t_2}\frac{K_N}{2C_L}dt = -\int_{V_1}^{V_2}\frac{dv_C}{[2(V_{DD}-V_{TN})-v_C]v_C}$$

$$\left(\int\frac{dx}{(a-x)x} = \int\frac{dx}{a(a-x)} + \int\frac{dx}{ax} = \frac{1}{a}\int\left[\frac{1}{a-x}+\frac{1}{x}\right]dx = \frac{1}{a}\ln\left(\frac{x}{a-x}\right)\right)$$

$$\left[V_2 = \frac{V_{DD}}{2},\ V_1 = V_{DD}-V_{TN}\right] \Rightarrow$$

$$\frac{K_N}{2C_L}(t_2-t_1) = -\frac{1}{2(V_{DD}-V_{TN})}\ln\left[\frac{v_C}{2(V_{DD}-V_{TN})-v_C}\right]\Bigg|_{V_{DD}-V_{TN}}^{V_{DD}/2}$$

⋮ algebra

$$= -\frac{1}{2(V_{DD}-V_{TN})}\ln\left[\frac{V_{DD}}{4V_{DD}-4V_{TN}-V_{DD}}\right]$$

$$(t_2-t_1) = \frac{C_L}{K_N(V_{DD}-V_{TN})}\ln\left[\frac{4(V_{DD}-V_{TN})-V_{DD}}{V_{DD}}\right]$$

$$= \frac{C_L}{K_N(V_{DD}-V_{TN})}\ln\left[\frac{4(V_{DD}-V_{TN})}{V_{DD}}-1\right]$$

$$(t_2-t_1) = R_{on}C_L\ln\left[\frac{4(V_{DD}-V_{TN})}{V_{DD}}-1\right]$$

$$t_{pHL} = (t_2-t_1)+(t_1-t_0) = (t_2-t_0)$$

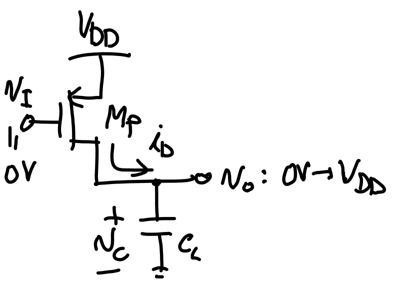
$$= R_{on}C_L\left\{\ln\left[\frac{4(V_{DD}-V_{TN})}{V_{DD}}-1\right]+\frac{2V_{TN}}{(V_{DD}-V_{TN})}\right\} = t_{pHL}$$

where $R_{on} = \dfrac{1}{K_N(V_{DD}-V_{TN})}$

$$t_{pHL} = R_{on}C_L \times f(V_{DD}, V_{TN})$$

t_{pLH}: output: $L \to H$

$\to$ connect C_L to V_{DD} $\to$ PMOS on, NMOS off



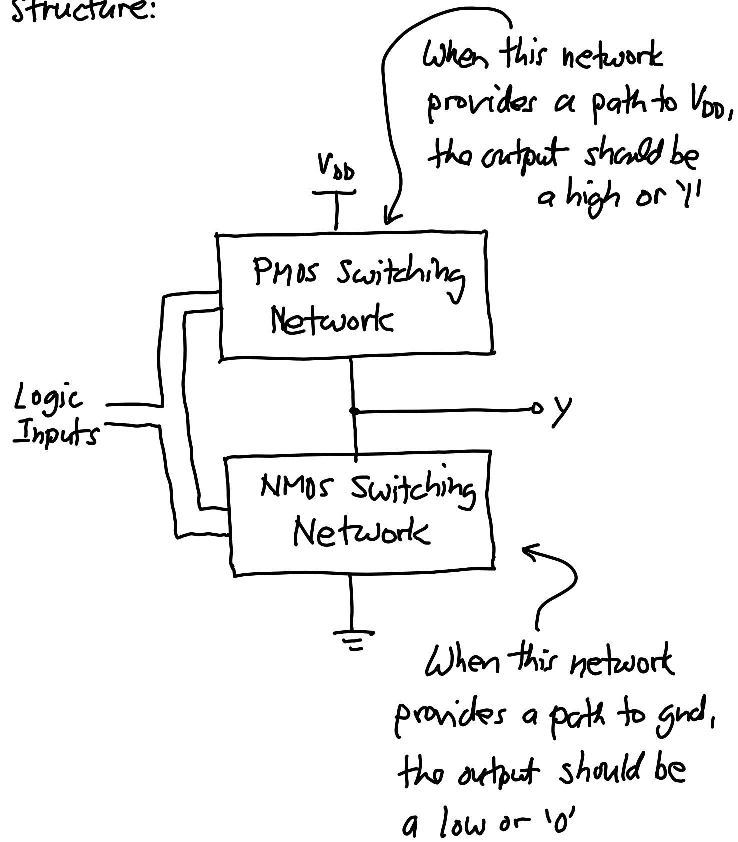
Through a similar analysis:

$$t_{pLH} = R_{on}C_L\left\{\ln\left[\frac{4(V_{DD}-|V_{TP}|)}{V_{DD}}-1\right]+\frac{2|V_{TP}|}{(V_{DD}-|V_{TP}|)}\right\}$$

$$t_p = \frac{t_{pLH}+t_{pHL}}{2}$$

Complex CMOS Gates

To realize more complex gates, use the following structure:



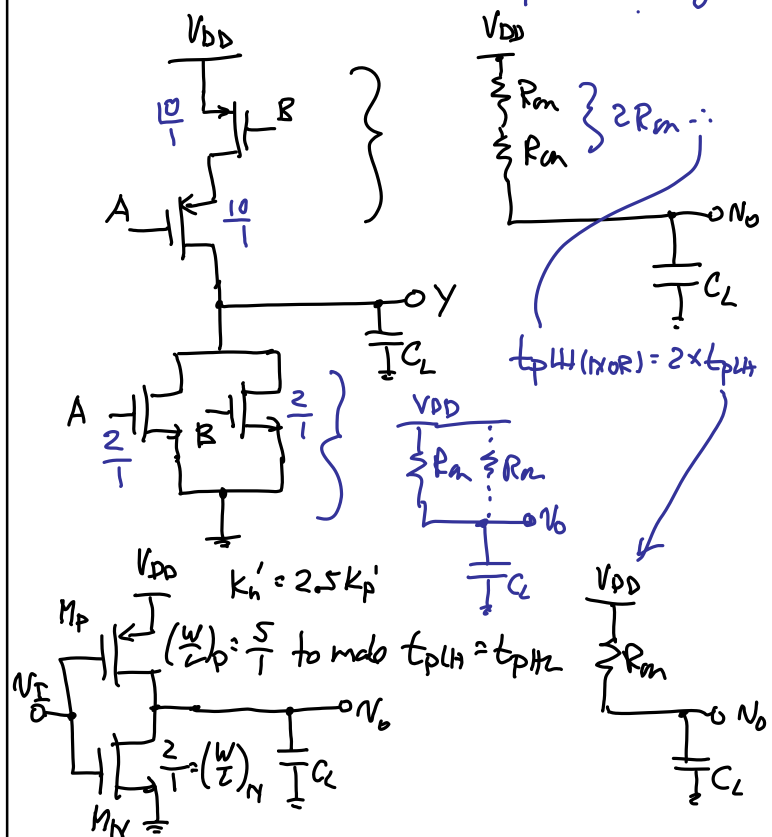
- For CMOS, to save power consumption, must avoid a conductive path connecting V_{DD} and ground in steady-state
- Otherwise, too much current will flow and dissipate power
- Should also minimize this path during transitions

CMOS NOR Gate

A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

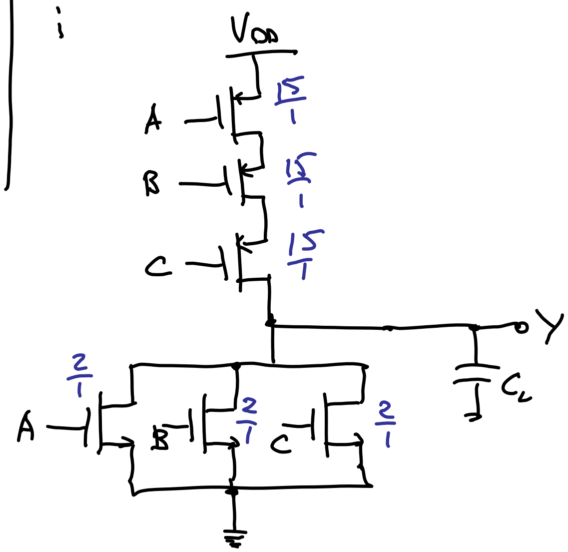
When both inputs are '0', there should be a path to V_{DD} ↳ '1'

Anytime there is a '1' in the input, need to pull down to gnd



How about 3 inputs (NOR)?

A	B	C	$Y = \overline{A+B+C}$
0	0	0	1
0	0	1	0
0	1	0	0
⋮	⋮	⋮	⋮



- What's Next?
- EE130: Semiconductor Devices
  - Did you like the physics parts? If so, then this is the course for you.
  - Will go much deeper and cover
    - Energy band diagrams
    - Short channel MOS
    - More accurate physical structure
    - Heterojunctions
    - Much more …
- EE143: Semiconductor Device Fabrication
  - Planar wafer-level fabrication methods that make IC's possible
  - Tools and chemistry
  - Process flow design
  - Hands-on wafer fabrication
- EE140: Analog Integrated Circuits
  - Supply and temperature independent biasing
  - Much larger circuits
  - Deeper understanding of op amps
  - Stability compensation
  - Feedback methods (by inspection)
- EECS151: Digital Integrated Circuits
  - Build upon propagation delay concepts
    - Short channel devices
  - Logic gates, adders, etc.
  - System-level design
    - Interconnect issues
    - Programmable arrays

- What's Next? (cont.)
- EE147: Microelectromechanical Systems (MEMS)
  - I'm biased, but … this is the coolest stuff, period!
  - Mechanics and Materials
  - Methods for fabricating tiny mechanics
  - Mechanical circuit design
  - You'll learn that all of your EE math skills and circuit techniques can just as easily be applied to mechanical devices and systems
  - Applications to sensing and RF