Lecture 40: Complex Gates

Announcements:
- Last lecture!
- HW#11 online and due during RRR week
- Lab 6 online and due 5 p.m., Friday, Dec. 7
- Labs will run as usual next week
- We will keep all normal office hours during RRR Week and Finals Week up through the Wednesday before the Final Exam
- There will be extra office hours during Finals Week, as explained in the Final Exam Info Sheet

Lecture Topics: (over the next few days)
- Complex CMOS Gates
- Final Exam Info Sheet

Last Time:
- Finished the expression for CMOS inverter $t_{pHL}$ propagation delay
- Now summarize this ...

[Diagram of CMOS inverter and propagation delay]
Case: $V_{OL} \geq V_{DD} - V_{TN} \rightarrow M_i$ Saturated

\[ i_D(t) = \frac{k_m}{2} (V_{GS} - V_{TN})^2 - C_L \frac{dV_c}{dt} \]

\[ dt = -\frac{2C_L dV_c}{K_N (V_{GS} - V_{TN})^2} - \frac{2C_L dV_c}{K_N (V_{DD} - V_{TN})^2} \]

\[ V_{OL} = V_{0L} = V_{DD} = V_{TN} \]

\[ \int_{t_0}^{t_1} dt = \int_{V_{DD} - V_{TN}}^{V_{DD} - V_{TN} - V_{LO}} \frac{2C_L}{K_N (V_{DD} - V_{TN})^2} (V_{DD} - V_{TN} - V_{LO}) \]

\[ (t_1 - t_0) = -\frac{2C_L}{K_N (V_{DD} - V_{TN})^2} (V_{DD} - V_{TN} - V_{LO}) \]

\[ \left( t_1 - t_0 \right) = \frac{2C_L}{K_N (V_{DD} - V_{TN})} \frac{V_{TN}}{V_{DD} - V_{TN}} = 2C_L R_m \frac{V_{TN}}{V_{DD} - V_{TN}} \]

Effective "on resistance" of the XNOR

\[ R_m = \frac{1}{K_N (V_{DD} - V_{TN})} \]

\[ v_m = \frac{1}{2} \left( V_{DD} - V_{TN} \right) \]

\[ v_m = \frac{V_{DD}}{2} \left( V_{DD} - V_{TN} \right) \]

\[ \frac{K_N}{2C_L} \left( t_1 - t_0 \right) = -\frac{1}{2} \ln \left( \frac{V_c}{V_{DD} - V_{TN}} \right) \]

\[ v_m = \frac{1}{2} \left( V_{DD} - V_{TN} \right) \]

\[ \frac{1}{4} \ln \left( \frac{V_{DD}}{V_{TN}} \right) \]

\[ \left( V_{DD} - V_{TN} \right) \]

\[ \frac{V_{DD} - V_{TN}}{V_{DD} - V_{TN} - V_{DD}} \]
(t_z - t_i) = \frac{C_L}{K_N(V_{dd} - V_{TN})} \ln \left[ \frac{4(V_{dd} - V_{TN}) - V_{DD}}{V_{DD}} \right] - 1 \right] 
(t_z - t_o) = R_{on}C_L \ln \left[ \frac{4(V_{dd} - V_{TN}) - V_{DD}}{V_{DD}} \right] - 1 \right] 
(t_{PHL}) = (t_z - t_i) + (t_z - t_o) \begin{align*}
&= R_{on}C_L \ln \left[ \frac{4(V_{dd} - V_{TN}) - V_{DD}}{V_{DD}} \right] + \frac{2V_{TN}}{(V_{dd} - V_{TN})} \right] 
&= t_{PHL} 
\text{WHERE} \quad R_{on} = \frac{1}{K_N(V_{dd} - V_{TN})} 
\Rightarrow 
\frac{1}{R_{on}} = K_N(V_{dd} - V_{TN}) 
\Rightarrow 
\frac{t_{PHL}}{R_{on}C_L} = \left( \frac{1}{V_{DD}} \right) \left( \frac{4(V_{dd} - V_{TN}) - V_{DD}}{V_{DD}} \right) + \frac{2V_{TN}}{(V_{dd} - V_{TN})} \right] 
\Rightarrow 
t_{PHL} = R_{on}C_L \times f(V_{dd}, V_{TN}) 

(t_{puh}) = \text{output: } L \rightarrow H 
\begin{align*}
\text{connect } C_L \text{ to } V_{DD} 
\text{PMOS on, NMOS off} 
\end{align*} 

V_{DD} 
\begin{align*}
\text{N}_L \quad M_p 
\text{GND} 
\text{GND} 
\text{N}_C \quad C_L 
\end{align*} 

\begin{align*}
\text{V}_o \quad \text{I}_o 
\end{align*} 

\text{N}_o: \text{OV} \rightarrow V_{DD} 

\text{N}_C: \text{OV} \rightarrow V_{DD} 

\text{t}_p = \frac{t_{puh} + t_{puh}}{2}
To realize more complex gates, use the following structure:

- For CMOS, to save power consumption, must avoid a conductive path connecting $V_{DD}$ and ground in steady-state.
- Otherwise, too much current will flow and dissipate power.
- Should also minimize this path during transitions.

**CMOS NOR Gate**

When both inputs are '0', there should be a path to $V_{DD}$.

Anytime there is a '1' in the input, need to pull down to ground.

$\text{PLH (NOR)} = 2 \times \text{PLH}$.
What's Next?

EE130: Semiconductor Devices

- Did you like the physics parts? If so, then this is the course for you.
- Will go much deeper and cover
  - Energy band diagrams
  - Short channel MOS
  - More accurate physical structure
  - Heterojunctions
  - Much more ...

EE143: Semiconductor Device Fabrication

- Planar wafer-level fabrication methods that make IC’s possible
- Tools and chemistry
- Process flow design
- Hands-on wafer fabrication

EE140: Analog Integrated Circuits

- Supply and temperature independent biasing
- Much larger circuits
- Deeper understanding of op amps
- Stability compensation
- Feedback methods (by inspection)

EECS151: Digital Integrated Circuits

- Build upon propagation delay concepts
  - Short channel devices
  - Logic gates, adders, etc.
  - System-level design
    - Interconnect issues
    - Programmable arrays
• What’s Next? (cont.)
• EE147: Microelectromechanical Systems (MEMS)
  ➤ I’m biased, but … this is the coolest stuff, period!
  ➤ Mechanics and Materials
  ➤ Methods for fabricating tiny mechanics
  ➤ Mechanical circuit design
  ➤ You’ll learn that all of your EE math skills and circuit techniques can just as easily be applied to mechanical devices and systems
  ➤ Applications to sensing and RF