Lecture 9: Vos and Input Bias Current

Announcements:
- HW#3 online and due Friday via Gradescope
- Lab#2 will be a two week lab
  - Prelab is due in the second week
  - But you should have proof of having started it when you go to lab this week
  - You will still do the lab this week and continue next week
- This Wednesday, 9/12: I will be out of town.
  - So no ground lecture that day
  - This is a video lecture

Lecture Topics:
- Input Offset Voltage
- Input Bias Current

Last Time:
- Started input offset voltage
- Now, continue with this

![Diagram of Input Offset Voltage, Vos](image)

Ideal Case: \( V_{os} = 0 \)
Reality: \( V_{os} \neq 0 \)
(usually, \( V_{os} \approx 1 \mu V - 5 \mu V \))

Model this with equivalent input offset voltage, \( V_{os} \):

Effect of \( V_{os} \) on Op Amp Clb:
Example: Non-Inverting Amplifier

\[ V_o = V_{os} \left(1 + \frac{R_2}{R_1}\right) \]

E.g., \( \frac{R_2}{R_1} = 9, V_{os} = 5\mu V \rightarrow V_o = 50 \mu V \)
(not so bad...)
**Example. Integrator**

\[ V_o = V_{os} + \frac{1}{C} \int_0^t V_{i}(t) \, dt \]

\[ V_o = V_{os} + \frac{1}{C} \int_0^t V_{os} \, dt \]

\[ V_o = V_{os}(1 + \frac{t}{RC}) + VCL_{t=0} \]

**Solution:** place resistor \( R_f \) in shunt with \( C \)

\( V_o = V_{os}(1 + \frac{R_f}{R}) \) prevents \( V_o \) from going to the rail!

**Input Bias Currents**

- Many op amps require small currents into their input transistor that allow the transistor to function.
- Currents are independent of \( R_{in} \)

\[ V_o = \frac{R_f}{R} \]

**Schematically:**

\[ I_{in} = I_{g1} + \frac{I_{os}}{2} \]

\[ I_{in} = I_{g2} - \frac{I_{os}}{2} \]

Average \( I_{in} \) value:

\[ I_{in} = \frac{I_{g1} + I_{g2}}{2} \] (typ. 100 nA for bipolar op amps)

Differential \( I_{in} \) value:

\[ I_{in} = |I_{g1} - I_{g2}| \] (typ. 10 nA for a bipolar op amp)

**Example. Non-Inverting Amplifier**

\[ V_o = \frac{R_2}{R_1} \left( I_{g1} + \frac{I_{os}}{2} \right) \]

\[ V_o = \frac{R_2}{R_1} \left( I_{g1} + \frac{I_{os}}{2} \right) \] not zero!

\[ \text{"virtual ground" current cannot flow through } R_1 \]
To reduce this effect: add resister to the (4) input

\[ i_z = I_{G1} - \frac{I_{B2} R_3}{R_1} \]

\[ V_o = -I_{B2} R_3 + R_2 \left( I_{G1} - \frac{I_{B2} R_3}{R_1} \right) \]

What value of \( R_3 \) makes \( V_o \to 0 \)?

Case \( I_{os} = 0 \): (i.e., \( I_{G1} = I_{B2} = I_{o1} \))

\[ V_o = I_{o1} \left( R_2 + R_3 \left( 1 + \frac{R_2}{R_1} \right) \right) \]

[For \( V_o = 0 \) \( \Rightarrow \]

\[ R_2 = R_3 \left( 1 + \frac{R_2}{R_1} \right) \rightarrow R_2 = \frac{R_2}{1 + \frac{R_2}{R_1}} = \frac{1}{R_1} + \frac{1}{R_2} \]

\[ \therefore P_3 = R_1 R_2 \rightarrow V_o = 0 \]

with \( I_{os} = 0 \)

Case \( I_{os} \neq 0 \): (i.e., \( I_{G1} = I_{o1} + \frac{I_{os}}{2} \), \( I_{B2} = I_{o1} - \frac{I_{os}}{2} \))

\[ V_o = -I_{B2} R_3 + R_2 \left( I_{G1} - \frac{I_{B2} R_3}{R_1} \right) \]

\[ V_o = -I_{B2} R_3 + R_2 \left( I_{G1} - \frac{I_{o1} R_3}{R_1} \right) \]

\[ R_3 = R_1 R_2 \]

\[ V_o = \frac{I_{o1} R_2}{2} \left( I_{B1} + \frac{I_{os}}{2} \right) R_2 \]

\[ \frac{10\mu A}{1\mu A} \sim 5\mu A \]

Setting \( R_3 = R_1 R_2 \) still helps even if \( I_{os} \neq 0 \).

Generalized Circuit Elements

<table>
<thead>
<tr>
<th>Resistor</th>
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<tbody>
<tr>
<td>Nonlinear Resistor</td>
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</tbody>
</table>

Linear Resistor

\[ i = \frac{v}{R} \]

Nonlinear Resistor

\[ i = f(v) \]
Capacitor

Linear Capacitance
\[ C = \frac{q}{V} \]

Nonlinear Capacitance
\[ C = f(V) \]

⇒ there are also nonlinear inductors → generally not seen in low-to-mid frequency integrated circuits.

Example: Diode – several models, all of which represent nonlinear resistors

A. Ideal

B. Constant Voltage

Diode "on" voltage → usually from 0.5 to 0.7 V

C. Actual Diode

\[ i = I_D(e^{V_{th}/I_T} - 1) \]

\[ V_T = 25 mV \]

\[ kT \]

\[ I_n \]

\[ n \]

Diode → not only a nonlinear resistor

⇒ also includes nonlinear capacitance

A more exact model for a diode would look like:

\[ Q = f''(V) = q\left(\frac{N_A N_D}{N_A + N_D}\right) AW_{P} \sqrt{1 + \frac{VR}{R'}} \]

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