Lecture 23: Small-Signal CE Amplifier Analysis

Announcements:
- HW#7 online and due Friday via Gradescope
- Lab#5 due Tuesday, Nov. 12, 5 p.m.
- Gave Z scores last time

Lecture Topics:
- Finish Common Emitter Amplifier
- Frequency Response
- High Frequency Model for BJT

Last Time:
- Going through a Common Emitter Amplifier small-signal analysis example
- Now, continue with this ...

Procedure for Small-Signal Analysis

For \( Q : \beta = 100, V_A = 100 \text{V} \):
Find the voltage gain, \( \frac{V_O}{V_S} \).
Draw the collector voltage waveform for:
\[
V_C = (0.014) \cos \omega t + 1V
\]

Source (Input)  Amplifier  Output Load

(Thevenin Equivalent)

\[
\begin{align*}
N_C &= V_C + N_S \\
N_O &= V_O + N_S
\end{align*}
\]
1. Determine the DC operating point
   - i.e., find the relevant DC voltages at all nodes and DC currents through all branches
2. Draw the DC circuit
   - Eliminate independent AC small-signal sources
     - Short AC voltage sources
     - Open AC current sources
   - Open all capacitors (in particular, open the bypass/coupling capacitors)
   - Use DC transistor models
     - this might entail nonlinearity in some cases, but approximations can alleviate

\[ V_{cc} = +12V \]
\[ R_2 = 30k \]
\[ R_3 = 3k \]
\[ C_e = 10\mu F \]
\[ R_E = 2.3k \]
\[ N_{C} = V_o + N_o \]
\[ V_{C} = V_0 + N_o \]
\[ N_{c1} = V_{c1} + N_{c1} \]
\[ N_{s1} = V_{s1} + N_{s1} \]

\[ N_{s} (DC) \]
\[ N_{s} (AC) \]

\[ V_{s} (DC) \]
\[ V_{s} (AC) \]

\[ V_{cc} = V_{cc}(DC) \]
\[ V_{c} = V_{c}(AC) \]

\[ R_S = 100 \]
\[ V_S = 1V \]
\[ R_1 = 30k \]
\[ R_2 = 10k \]
\[ R_E = 2.3k \]

\[ R_{BB} = R_1/R_2 = (10k)/(30k) = 7.5k \]

\[ V_{BB} = V_{cc}(R_2/(R_1+R_2)) = (12)V(30k)/(40k) = 3V \]
② Determine the elements in the small-signal transistor model(s)
   - If more than one transistor, might need to determine SS element values for several of them
   
   \[
   I_{C} = \frac{V_{BB} - V_{FE}}{R_{E} + \frac{R_{BB}}{\beta}} = \frac{3 - 0.7}{2.3k + \frac{7.5K}{100}} = 0.97mA \approx 1mA
   \]
   \[
   I_{B} = \frac{I_{C}}{\beta} = 0.01mA
   \]
   \[
   V_{B} = V_{BB} - I_{B}R_{BB} = 3 - (0.01m)(7.5k) = 2.92V
   \]
   \[
   V_{E} = 2.92 - 0.7 = 2.22V
   \]
   \[
   V_{C} = V_{CC} - I_{C}R_{C} = 12 - (1m)(3k) = 9V
   \]

   Faster Way:
   - Ignore \( I_{B} \) → \( V_{B} = V_{BE}(\frac{R_{E}}{R_{E} + R_{C}}) = 3V \)
   - \( V_{E} = V_{B} - V_{BE} = 3 - 0.7 = 2.3V \)
   - \( I_{E} = \frac{V_{E}}{R_{E}} = 1mA = I_{C} \)
   - \( I_{B} = \frac{I_{C}}{\beta} = 0.01mA \)
   - \( V_{C} = V_{CC} - I_{C}R_{C} = 9V \)

   \[
   I_{RIN} = \frac{V_{CC}}{R_{E} + R_{C}} = 0.3mA > 10I_{B}
   \]
   For a stable bias point.

③ Obtain the small-signal circuit
   - Eliminate independent DC sources
     - Short DC voltage sources
     - Open DC current sources
   - Short large coupling capacitors (\( C' > 10\mu F \))
   - Use small-signal transistor models

![Circuit Diagram]
Use standard circuit analysis (i.e., KCL or KVL with superposition) to determine the parameters of interest.

- Gain, $A_v$
- Input Resistance, $R_i$
- Output Resistance, $R_o$
- Low Frequency Cut-off, $\omega_b$
- High Frequency Cut-off, $\omega_h$

Determine all of these during small-signal analysis.

The total gain of the simplified amplifier circuit takes the form:

$$\frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} \cdot A_N \cdot \frac{R_i}{R_i + R_L}$$

For ideal worst: $R_i = \infty$ $\quad R_o = 0$

$(R_i \gg R_L)$ $(R_o \ll R_L)$

**Amplifier Gain**

$$A_N = \left| \frac{V_o}{V_i} \right|_{R_i=\infty} (a_i=0)$$

$$A_N \approx \frac{g_m (R_i R_L)}{R_L}$$

$$A_N \approx -g_m R_C$$

$$R_o \gg R_C$$
For the total clct:

\[ G_{\text{in}} = \frac{V_{\text{in}}}{V_{\text{out}}} = \frac{R_c}{R_c + R_L} \]

\[ = \frac{g_m R_L}{g_m R_L + R_s} \cdot \left( \frac{R_c}{R_c + R_L} \right) \]

\[ = - \frac{g_m R_L}{g_m R_L + R_s} \cdot g_m (R_c R_L) \]

\[ = - \frac{18.75}{18.75 + 100} \cdot (0.04) \cdot (3 \times 115K) \]

\[ = -71.2 : \frac{N_o}{N_s} \text{ (midband gain)} \]

\[ = \text{just Fax tricks...} \]

\[ \text{Short clct: Current Gain for the C.E. amp} \]

\[ g_m \left( R_{\text{in}}/R_L \right) \left( \begin{array}{c} \text{at} \ R_L = 0 \\
\text{and} \ N_o = 0 \end{array} \right) \]

\[ \text{at} \ R_L = 0 \]

\[ = g_m R_L \]

\[ \text{at} \ N_o = 0 \]

\[ = g_m R_L \]

\[ \text{At} \ R_L = 0 \]

\[ = g_m R_L \]

\[ A_{\text{in}} = g_m (R_{\text{in}}/R_L) \]

\[ A_{\text{in}} = g_m R_L \]

\[ A_{\text{in}} = g_m R_L \]

\[ \text{At} \ R_L = 0 \]

\[ = g_m R_L \]

\[ A_{\text{in}} = g_m R_L \]
Use the gain and resistances determined above to obtain the small-signal voltages and currents at each node/branch of the circuit.

- To obtain the actual node & branch signals, superpose the DC and small-signal AC solutions.
An Inking of Inspection Analysis

- for for s.s. ckt analysis:

\[ \frac{N_o}{V_o} = \frac{N_i}{V_i}, \quad \frac{N_o}{N_o} = \frac{V_{T+}+V_{be}+V_{T-}}{g_m(V_{T+}+V_{be}+V_{T-})} \]

... but more later...