SOLUTIONS TO 2nd MIDTERM

Problem 1 of 3 Answer each question briefly and clearly. (30 points)

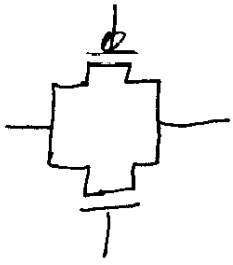
How is the voltage gain of a CMOS inverter related to the transconductances of its transistors? (5pts)

$$A_V = -(g_{mn} + g_{mp})(r_{on} // r_{op})$$

Why are CMOS NAND gates preferable to CMOS NOR gates? (5pts)

CMOS NAND uses p-channel transistors in parallel. CMOS NOR uses them in series, and that makes them too big, → CMOS NOR takes more space than CMOS NAND.

Why do you need an n-channel *and* a p-channel transistor in parallel in order to have a proper "pass" logic gate? (5pts)



the n-channel can "pass" anything from 0V to $V_{DD} - V_{tn}$. The p-channel can pass $-V_{tp}$ to V_{DD}. You need both to pass 0 to Vdd.

What is a "unilateral" amplifier?(5pts)

R_{in} independent of R_L

R_{out} independent of R_S

Please indicate with an up or down arrow the effect of the following on the voltage gain (Av) of a common source amplifier (5 pts)

Parameter	Effect on Av	Brief Explanation (optional)
W/L ↑	↑	since ↑ $g_m = \frac{W}{L}\mu_n C_{ox}(V_{GS}-V_{tn}) = \sqrt{2(\frac{W}{L})\mu_n C_{ox} I_D}$
Idsat ↑	↓	$g_m \uparrow \propto \sqrt{I_{dsat}}$, but $r_o \downarrow \propto \frac{1}{I_{dsat}}$
L ↑	↑	$g_m \downarrow \propto \sqrt{1/L}$ $r_o \uparrow \propto L$
$\mu_n C_{ox}$ ↑	↑	$g_m \uparrow \propto \sqrt{\mu_n C_{ox}}$

$$A_V = -g_m(r_o // r_{oc})$$

What single-transistor amplifier stage can be used to ensure very high output resistance? (5pts)

common base
common gate
} i.e. current buffers.

Problem 2 of 3 (35 points)

In this problem you will size a CMOS inverter with process parameter V_{Tn}= 0.7V, V_{Tp}= -0.9V, $\mu_n Cox = 50\mu A/V^2$, $\mu_p Cox = 25\mu A/V^2$, $\lambda_n = \lambda_p = 0.1V^{-1}\mu m$ ~~2~~ typo. Assume equal lengths and V_{DD}=5V.

For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

a) Calculate the ratio W_n/W_p, such that $V_M = 2.5V$ (for this question you can ignore the channel-lenght modulation effect). (7pts)

$$V_M = \frac{V_{Tn} + \sqrt{\frac{K_p}{K_n}}(V_{DD}+V_{Tp})}{1+\sqrt{\frac{K_p}{K_n}}}$$

$$V_M + V_M\sqrt{\frac{K_p}{K_n}} = V_{Tn} + \sqrt{\frac{K_p}{K_n}}(V_{DD}+V_{Tp})$$

$$V_M - V_{Tn} = (V_{DD}+V_{Tp}-V_M)\sqrt{\frac{K_p}{K_n}}$$

$$\sqrt{\frac{K_n}{K_p}} = \frac{V_{DD}+V_{Tp}-V_M}{V_M - V_{Tn}}$$

$$\sqrt{\frac{K_n}{K_p}} = \sqrt{\frac{\left(\frac{W}{L}\right)_n \mu_n C_{ox}}{\left(\frac{W}{L}\right)_p \mu_p C_{ox}}} = \sqrt{2\cdot\frac{W_n}{W_p}}$$

$$\sqrt{2\cdot\frac{W_n}{W_p}} = \frac{V_{DD}+V_{Tp}-V_M}{V_M - V_{Tn}}$$

$$\frac{W_n}{W_p} = \frac{1}{2}\left(\frac{V_{DD}+V_{Tp}-V_M}{V_M - V_{Tn}}\right)^2$$

$$\frac{W_n}{W_p} = \frac{1}{2}\left(\frac{2.5-.9}{2.5-.7}\right)^2$$

$$= .395$$

b) When $V_{in} = V_M$ we want the current through the inverter to be 1mA. What is W_n and W_p assuming that the channel length of both devices is 2µm? (7pts)

$$I_D = \frac{1}{2}\left(\frac{W}{L}\right)_n \cdot \mu_n C_{ox}(V_M - V_{Tn})^2$$

in sat because $V_{DS} > V_{GS} - V_{Tn}$

$$2.5 > 2.5 - .7$$

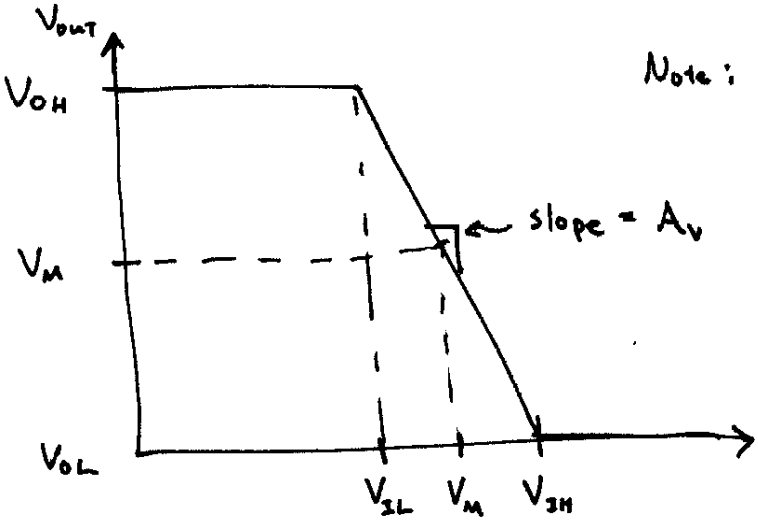
$$W_n = \frac{2\cdot L\cdot I_D}{\mu_n C_{ox}(V_M - V_{Tn})^2}$$

$$= \frac{2(2\,\mu m)(1\times10^{-3}A)}{\left(50\frac{\mu m}{V^2}\right)(2.5-.7)^2} = 24.7\,\mu m$$

$$W_p = W_n\left(\frac{W_p}{W_n}\right)$$

$$= (24.7\,\mu m)\left(\frac{1}{.395}\right) = 62.5\,\mu m$$

c) Sketch and label the voltage transfer characteristic with V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_M.(7pts)



Note: piecewise linear approximation is ok for CMOS inverter.

$$g_{mn} = \sqrt{2 \cdot \mu_n C_{ox} \cdot \frac{W_n}{L_n} \cdot I_D}$$

$$g_{mp} = \sqrt{2 \cdot \mu_p C_{ox} \cdot \frac{W_p}{L_p} \cdot I_D}$$

$$r_{on} = \frac{1}{\lambda_n I_D}$$

$$r_{op} = \frac{1}{\lambda_p I_D}$$

$$A_v = -(g_{mn} + g_{mp})(r_{on} \parallel r_{op})$$

d) What are the values of NM_L and NM_H? (7pts)

$$V_{IL} = V_m - \frac{(V_{DD} - V_m)}{A_v}$$

$$V_{IH} = V_m - \frac{V_m}{A_v}$$

$$N_{MH} = V_{OH} - V_{IH}$$

$$N_{ML} = V_{IL} - V_{OL}$$

for my $\frac{W}{L}$ values, and $\lambda = 0.1$,

$g_{mn} = 1.14 \cdot 10^{-3}$ S

$g_{mp} = 1.25 \cdot 10^{-3}$ S

$r_{on} = r_{op} = 10$ kΩ

$A_v =$ [redacted] -11.96

$NM_L = V_{IL} = 2.29$V $V_{IH} = 2.71$V $NM_L = 2.29$V

e) Would the noise margins improve if you made the devices longer, while keeping everything else fixed? (Give a yes/no answer and explain it in brief, qualitative terms) (7pts)

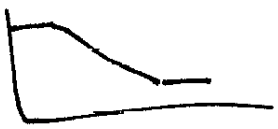
assuming symmetrical inverter for simplicity,

$$g_m = \mu C_{ox} \frac{W}{L} (V_m - V_T)$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{\lambda \cdot \mu C_{ox} \frac{W}{L} (V_m - V_T)^2}$$

so $A_v = g_m r_o = \frac{1}{\lambda (V_m - V_T)}$ ← const.

Since $\lambda \propto \frac{1}{L}$, $A_v \propto L$.

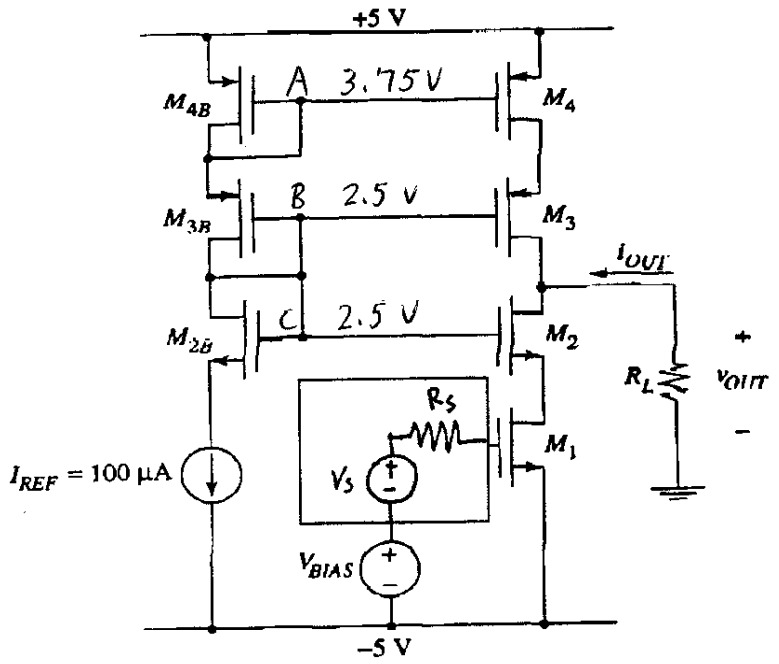


low A_v, low NM.

high A_v, high NM

Therefore, increasing L increases A_v, which improves noise margins.

Problem 3 of 3 (35 points)



$V_{Tp} = -0.7$ V
$\mu_p C_{ox} = 25\ \mu A/V^2$
$\lambda_p = 0.05\ V^{-1}$

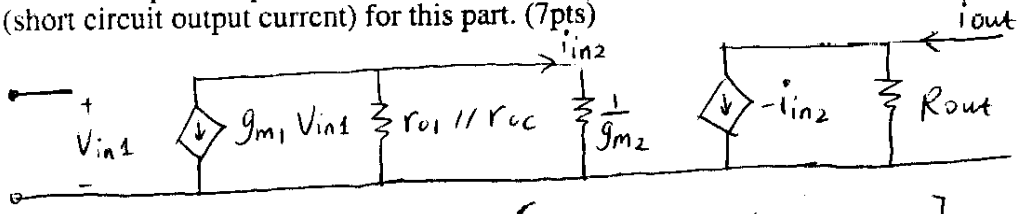
$V_{Tn} = 0.7$ V
$\mu_n C_{ox} = 50\ \mu A/V^2$
$\lambda_n = 0.07\ V^{-1}$

$M_2 = M_{2B} = 40/1.5$
$M_3 = M_{3B} = 40/1.5$
$M_4 = M_{4B} = 40/1.5$

A CMOS cascode transconductance amplifier and the device data are shown above. There is no backgate effect.

For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

(a) Find the $(W/L)_1$ for M_1, so that the small signal transconductance i_{out}/v_s = 1mS. Assume R_L=0Ω (short circuit output current) for this part. (7pts)



Where $R_{out} = \left[\left(\frac{r_{o2}}{2} + g_{m2} r_{o2} (r_{o1} // r_{oc})\right)\right] // r_{oc}$

Soure resistance to the CG-stage

$r_{oc} = (1 + g_{m3} r_{o4}) r_{o3}$

Ignore the interstage loss, then $G_m = g_{m1} = \sqrt{2 \left(\frac{W}{L}\right)_1 \mu_n C_{ox} I_{D1}}$

$I_{D1} = \frac{(W/L)_4}{(W/L)_{4B}} I_{REF} = I_{REF} = 100\ \mu A$

$\therefore \left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{2 \mu_n C_{ox} I_{D1}} = \frac{(1m)^2}{2 \times 50\mu \times 100\mu} = 100$

(b) Calculate the value of V_{BIAS} using the $(W/L)_1$ calculated in part (a) such that $I_{out} = 0A$. (7pts)

Note $I_{D_1} = I_{REF} = 100\ \mu A$ if $I_{out} = 0$

$$I_{D_1} = \left(\frac{W}{2L}\right)_1 \mu_n C_{ox} \cdot (V_{GS1} - V_{Tn})^2$$

$$V_{GS1} = V_{Tn} + \sqrt{\frac{2I_{D_1}}{\left(\frac{W}{L}\right)_1 \mu_n C_{ox}}} = 0.7 + \sqrt{\frac{2 \times 100\mu}{100 \times 50\mu}}$$

$$= 0.9\,V$$

$\therefore$ $V_{BIAS} = 0.9\,V$

(c) Calculate the output resistance of this transconductance amplifier. (7pts)

$$r_{oc} = (1 + g_{m3} r_{04}) r_{03}$$

$$g_{m3} = \sqrt{2 \left(\frac{W}{L}\right)_3 \mu_p C_{ox} \cdot (-I_{D_3})} = \sqrt{2 \times \frac{40}{1.5} \times 25\mu \times 100\mu} = 365\,\mu S$$

$$r_{04} = r_{03} = \frac{1}{\lambda_p (-I_{D3})} = \frac{1}{0.05 \cdot 100\mu} = 200k\Omega$$

$$r_{oc} = (1 + 365\mu \cdot 200k) \cdot 200k = 14.8\,M\Omega$$

Note $R_{out} = \left[r_{o2} + g_{m2} r_{o2} (r_{o1} \,//\, r_{oc})\right] \,//\, r_{oc}$

$$r_{o1} = r_{o2} = \frac{1}{\lambda_n I_{D_1}} = \frac{1}{0.07 \times 100\mu} = 143\,k\Omega$$

$\therefore$ $r_{oc} >> r_{o1}$

$$R_{out} \simeq (r_{o2} + g_{m2} r_{o2} r_{o1}) \,//\, r_{oc}$$

$$g_{m2} = \sqrt{2 \left(\frac{W}{L}\right)_2 \cdot \mu_n C_{ox} \cdot I_{D_2}} = \sqrt{2 \times \frac{40}{1.5} \times 50\mu \times 100\mu} = 516\,\mu S$$

$$R_{out} = (143k + 516\mu \times 143k \times 143k) \,//\, 14.8M$$

$$= 6.21\,M\Omega$$

(d) What is the maximum value of the load resistor R_L at which the overall transconductance is degraded by 20% from the original value of 1mS? (7pts)

Overall $\frac{i_{out}}{V_S} = G_M \cdot \frac{R_{out}}{R_{out}+R_L}$

Want $\frac{R_{out}}{R_{out}+R_L} \geq 0.8$

$\therefore \quad R_L \leq 1.55\,M\Omega$

(e) Calculate the maximum voltage swing at the output of this amplifier. (7pts)

First, compute voltages at point A, B and C. (see Graph)

$-I_{D4B} = \left(\frac{W}{2L}\right)_{4B} \cdot \mu_p C_{ox} \left(V_{SG_{4B}} + V_{Tp}\right)^2$

$V_{SG_{4B}} = \sqrt{\frac{-I_{D4B}}{\left(\frac{W}{2L}\right)_{4B} \mu_p C_{ox}}} - V_{Tp}$

$= \sqrt{\frac{100\,u}{\frac{40}{2\times1.5} \cdot 25u}} + 0.7 = \sqrt{\frac{3}{10}} + 0.7 = 1.25\,V$

$\therefore \quad V_A = 5 - 1.25 = 3.75\,V.$

$V_B = 3.75 - 1.25 = 2.5\,V$

$V_C = V_B = 2.5\,V$

We need to keep M_3 and M_2 in saturation

$V_{DS3} \geq V_{GS3} - V_{Tn} \Rightarrow V_{out} \geq 2.5 - 0.7 = 1.8\,V$

$V_{SD4} \geq V_{SG4} + V_{Tp} \Rightarrow V_{out} \leq 2.5 + 0.7 = 3.2\,V$

$\therefore \quad V_{out,min} = 1.8\,V, \quad V_{out,max} = 3.2\,V$