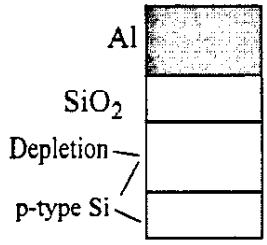
FINAL SOLUTIONS

Problem 1 of 4: Answer each question briefly and clearly. (3 points each, total 24)

What type of electrical current (drift or diffusion?) and what type of carriers (holes or electrons?) flows between the source and the drain of an n-channel MOS transistor?

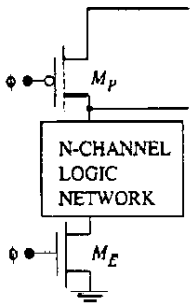
drift (because it is caused by an E-field)
electrons (because it is an n-channel)

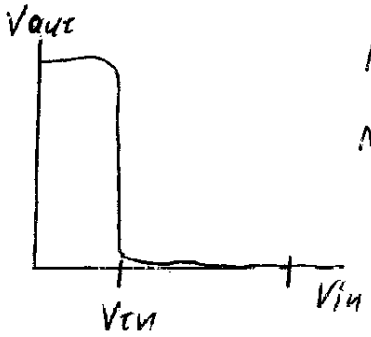
Where is the *maximum* absolute electric field within an MOS capacitor in depletion, made of Al, SiO_2 and p-type doped Silicon? (Mark your answer on the graph and give brief explanation)



← here, because SiO_2 has the lowest dielectric constant.

What are the noise margins of a dynamic logic gate that employs an n-channel logic network?





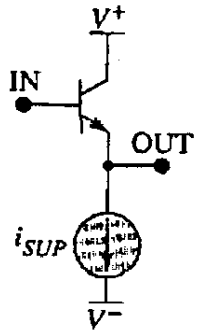
$NMH = V_{DD} - V_{tn}$

$NML = V_{tn}$

What physical aspect of a planar bipolar transistor determines its Early Voltage value?

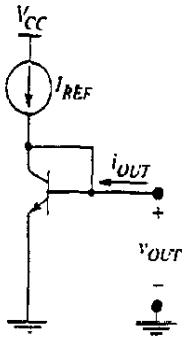
The width of the base (through the phenomenon known as "base-width" modulation)

Is it important to build a current supply source with an *extremely* high output resistance when biasing a common collector amplifier? Explain your answer.



No. Rout was supposed to be small, so it does not care.
(Rin was supposed to be large, but it is going to be dominated by RL anyway).

What can a circuit designer do to adjust the output voltage of the following npn bipolar diode-connected voltage source?



A typical value for this voltage source is about: ~0.7V

To reduce this value, the designer must:

decrease IREF, or increase Is (make transistor bigger)

To increase this value the designer must:

do the opposite of above

What single-stage amplifiers suffer from the so-called "Miller effect" that limits their frequency response?

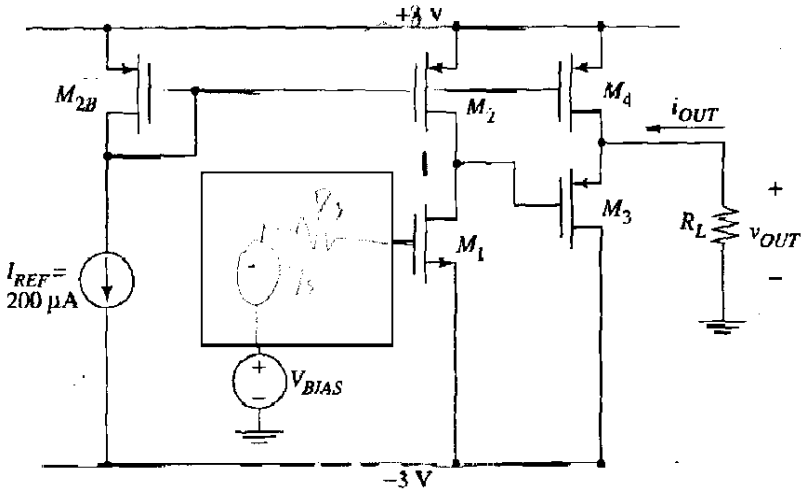
CE, CS (because they amplify)

What is the definition of the common-mode rejection ratio of a differential amplifier?

$$CMRR = \frac{\text{Gain in differential mode}}{\text{Gain in common mode.}}$$

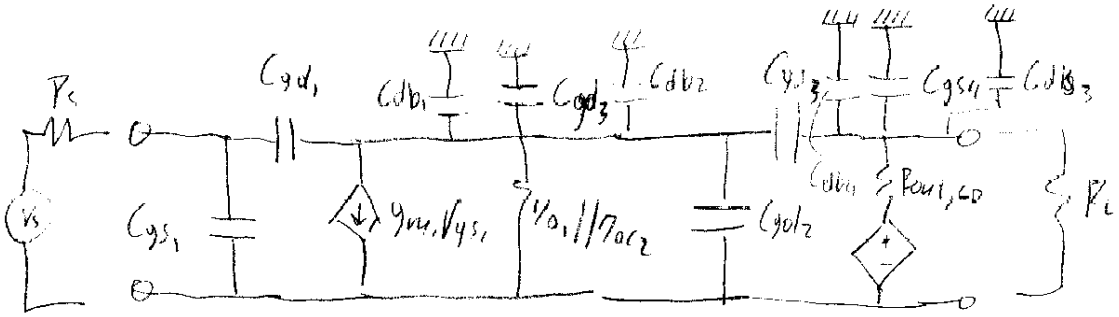
Problem 2 of 4 (26 points)

Below is given a voltage amplifier with $(W/L)_1 = 50/2$, $(W/L)_3 = 100/2$ and $(W/L)_{2B} = (W/L)_2 = (W/L)_4 = 50/4$. Assume that all backgates are shorted to their respective sources. Assume that V_{BIAS} is set such that all devices are operating in their constant current region.



For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

a) Draw the small signal model for the CS-CD stages, including parasitic capacitances. (5 points)



b) Draw the two-port model of this CS-CD stage and calculate the following parameters: A_V (i.e. unloaded DC voltage gain of the entire amplifier), Rin and Rout. Also calculate the DC voltage gain v_{out}/v_s when $R_s = 5k\Omega$ and $R_L = 500\Omega$. (5 points)

$g_{m_2} = 707\mu S$

$g_{m_1} = 707\mu S \quad r_{o_1} = (\lambda_n I_{sup})^{-1} = (0.05 \cdot 700\mu A)^{-1} = 100k\Omega$

$A_V = -g_{m_1}(r_{o_1} // r_{o_2}) = -47.1\ V/V$

$r_{o_2} = r_{o_1} = (0.05 \cdot 700\mu)^{-1} = 200M\Omega\ (L = 4\mu m)$ ~~$= 70\Omega$~~

$R_{in} \to \infty \quad R_{out} = g_{m_2}^{-1} = 1.41M\Omega$

$\frac{v_{out}}{v_s} = A_V\left(\frac{R_L}{R_L + R_{out}}\right) = -17.3\ V/V$

c) Find the ω_{3db} for this amplifier using the method of open-circuit time constants. (Hint #1: make sure that you include these parasitic capacitances: C_{gs1}, C_{gd1}, C_{db1}, C_{db2}, C_{gd3}, C_{gs3}, C_{db3} and C_{db4}. Hint #2: all these capacitances combine to *five* distinct capacitances, for which you will then have to calculate the open circuit time constants.) Answer this question in the following four steps:

c1) From part (a), combine all these capacitances to the following five, and calculate their values. (3 points)

$C_{gs1} = \frac{2}{3} W_1 L_1 C_{ox} + C_{ov1} W_1 = \frac{2}{3} \times 50 \times 2 \times 2.3 + 50 \times 0.5 = \boxed{178\,fF}$

$C_{gd1} = W_1 C_{ov1} = \boxed{25\,fF}$

C_1 (capacitance between ground and node "1") $= C_{db1} + C_{gd3} + C_{db2} + C_{gd2} = 61 + 112 + 50 + 25 = \boxed{248\,fF}$

$C_{db1} = W_1 L_{diff_n} C_{j_n} + (W + 2L_{diff_n}) C_{jsw_n} = 50 \times 6 \times 0.1 + (50 + 12) \times 0.5 = 61\,fF$

$C_{db2} = C_{db4} = 50 \times 6 \times 0.3 + (50 + 12) \times 0.35 = 112\,fF$

$C_{gd3} = 100 \times 0.5 = 50\,fF \qquad C_{gd2} = 25\,fF$

$C_{gs3} = \frac{2}{3} W_3 L_3 C_{ox} + W_3 C_{ov_p} = \frac{2}{3} \times 100 \times 2 \times 2.3 + 100 \times 0.5 = \boxed{357\,fF}$

$C_L = C_{db4} + C_{gs4} + C_{db3} = 112 + 332 + 219 = \boxed{663\,fF}$

$C_{gs4} = \frac{2}{3} \cdot 50 \times 4 \times 2.3 + 50 \times 0.5 = 332\,fF$

$C_{db3} = 100 \times 6 \times 0.3 + (100 + 12) \times 0.35 = 219\,fF$

c2) Calculate the resistance "seen" by each of the above capacitances. (2 points)

$R_{T\,gs1} = R_S = \boxed{5k}$ $\qquad R_{T\,gd1} = R_S + r_{o1} \| r_{oc2} + g_{m1} r_{o1} \| r_{oc2} \cdot R_S$

$= 5k + 66.7k + 0.907m \cdot 5k \cdot 66.7k$

$= \boxed{307\,k\Omega}$

$R_{T1} = r_{o1} \| r_{oc2} = \boxed{66.7\,k\Omega}$

$R_{T\,gs3} = (r_{o1} \| r_{oc2}) \left(1 - \frac{R_L}{\frac{1}{g_{m3}} + R_L}\right) + \frac{1}{g_{m3}} \| R_L$

$= 66.7k \left(1 - \frac{500}{1.41k + 500}\right) + 1.41k \| 500 = \boxed{49.6\,k\Omega}$

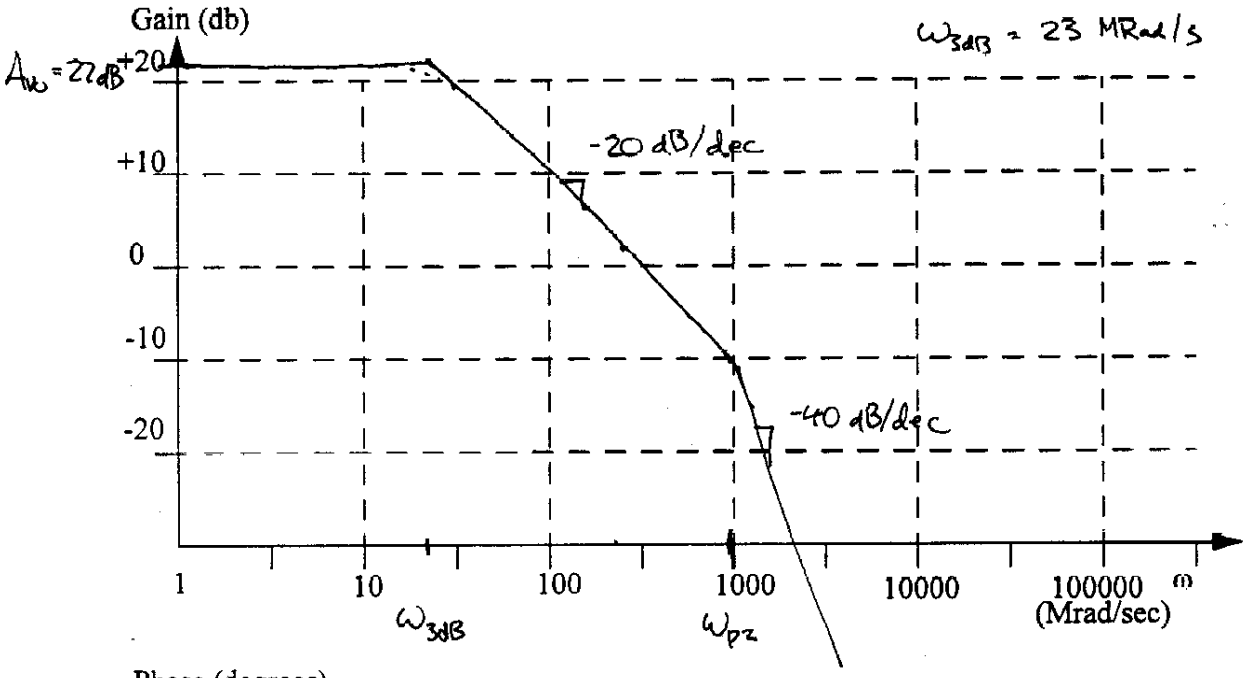
c3) Calculate the dominant pole for the circuit. (1 point) $R_{T,L} = R_L \| \frac{1}{g_{m3}} = \boxed{369\Omega}$

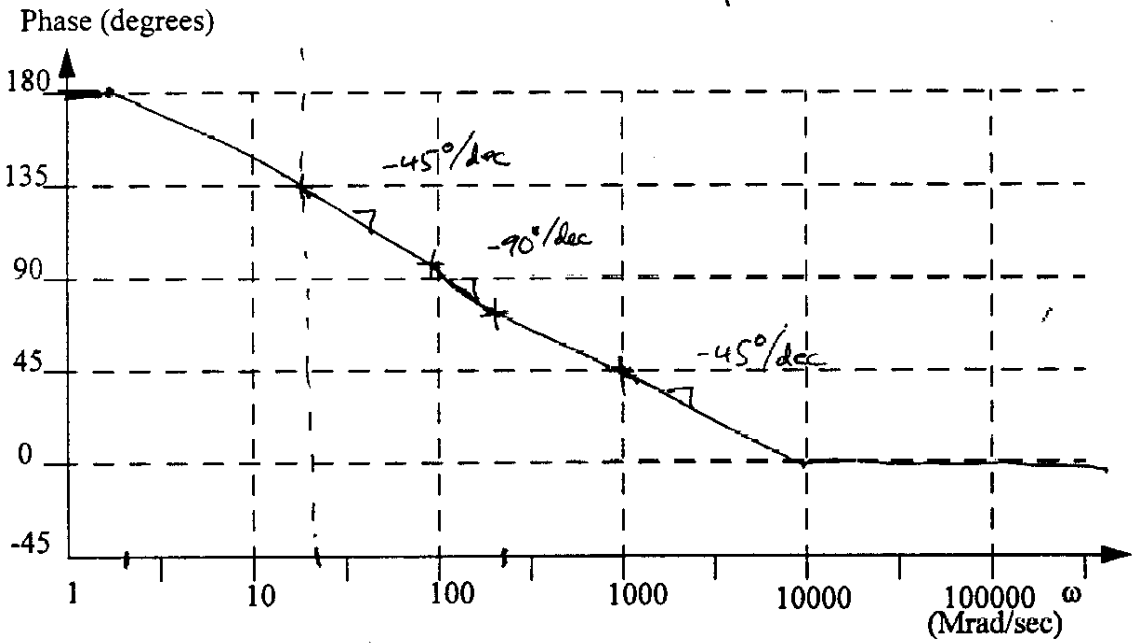
$\Sigma\tau = 178f \times 5k + 25f \times 307k + 248f \times 66.7k + 357f \times 49.6k + 663f \times 0.369 = 43.06\,ns$

$\omega_{3dB} \cong \frac{1}{\Sigma\tau} = 23\,M\,rad/s$

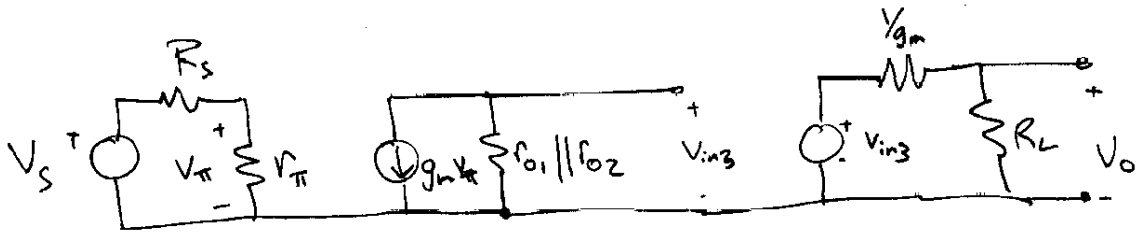
d) Assuming that, in addition to the dominant pole you found in part c, this amplifier has a *second* pole at 1000Mrad/sec, draw the amplitude and phase diagrams. (5 points)
If you could not find the loaded DC voltage gain in (b), assume it is -20V/V and check here: ☐
If you could not find the dominant pole ω_{3db} in (c), assume it is 30Mrad/s and check this box: ☐

$A_{vo} = -12$ mag $|A_{vo}| = 20 \log(12) = 22$dB phase $\angle A_{vo} = 180°$





e) Quite frankly, this is not a very good amplifier, so go ahead and replace M_1 with an npn bipolar transistor, redraw the circuit and calculate the new loaded DC voltage gain. (5 points)



$$\frac{V_o}{V_S} = \frac{r_\pi}{r_\pi + R_S} \cdot -g_{m1}(r_{o1} \| r_{o2}) \cdot \frac{R_L}{R_L + 1/g_{m2}}$$

$R_S = 5k$

$R_L = 500\Omega$

$$g_{m1} = \frac{200\mu A}{.0259} = .0077\ S$$

$$r_\pi = \frac{\beta}{g_{m1}} = \frac{100}{.0077} = 13\ k$$

$$r_{o1} = \frac{V_A}{I_c} = \frac{25V}{200\mu A} = 125k$$

$\lambda = 0.1\ V^{-1}\cdot\mu m / 4\mu m$

$\lambda = .025\ V^{-1}$

$$r_{o2} = \frac{1}{\lambda I_D} = \frac{1}{(.025)(200\mu)} = 200k$$

$$g_{m2} = \sqrt{2K'\frac{W}{L} I_D} = \sqrt{2 \cdot 25 \cdot 10^{-6} \cdot 50 \cdot 200\mu A}$$

$$= 707\mu S = (1414)^{-1}$$

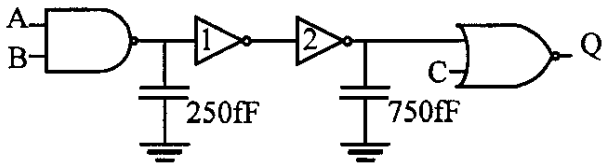
$$A_V = \frac{13k}{18k} \cdot -.0077 \cdot \left(\frac{200k \cdot 125k}{200k + 125k}\right) \cdot \frac{500}{500 + 1414}$$

$$\boxed{A_V = -111.7}$$

Problem 3 of 4 (25 points)

Consider the following static CMOS logic circuit. The two capacitances on the schematic represent the capacitance of the wiring connecting these gates.

For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

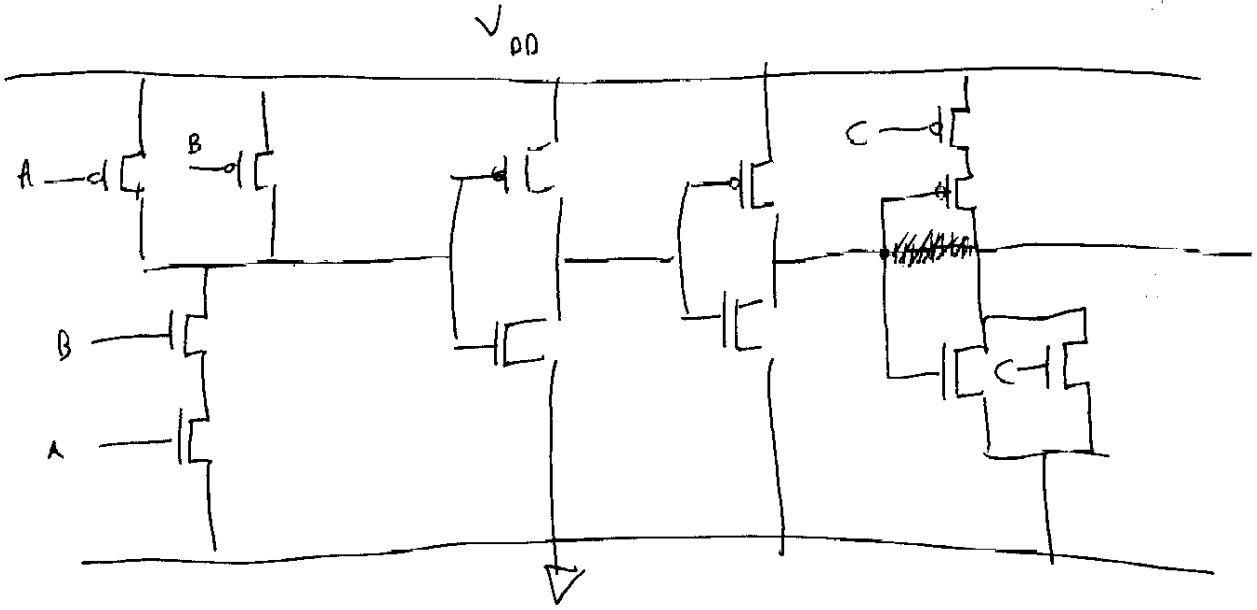


a) Write the logical expression for Q in terms of A, B and C, and fill out the truth table. (3 points)

Q = $A B \overline{C}$

A	B	C	Q
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	0
0	1	1	0
1	0	1	0
1	1	1	0

b) Re-draw this circuit showing all the transistors that implement the logical functions depicted above in CMOS static logic, using a 5V supply voltage. (4 points)



c) All transistors have a channel length L=2μm. The widths of the n-channel transistors for the inverters and logic gates are as follows:
NAND gate: $W_n = 4\mu m$, Inverter 1: $W_n = 6\mu m$, Inverter 2: $W_n = 18\mu m$, NOR gate: $W_n = 4\mu m$.
Determine the widths of the p-channel transistors in the circuit such that the inverters have equal propagation delays $t_{PHL} = t_{PLH}$ and that the logic gates have equal worst-case propagation delays. (6 points)

Inv_1 : $W_{p_1} = 12\ \mu m$

Inv_2 : $W_{p_2} = 36\ \mu m$

NAND: $W_p = 4\ \mu m$

NOR: $W_p = 12\ \mu m$

d) Find the numerical value of the worst-case propagation delay t_p for the NAND gate. The drain-bulk capacitances can be neglected because of the large wire capacitance. (But do take into account the effect of the gate capacitance through C_{ox}!)(6 points)

$$t_{pLH} = \frac{(C_w + C_G)\left(V_{DD}/2\right)}{\frac{1}{2}\left(\frac{W}{2L}\right)\mu_n C_{ox}\left(V_{DD}-V_{Tn}\right)^2}$$

↳ numbers in basics!

$$C_G = C_{G\,inv1} = C_{ox}\left(W_n L_n + W_p L_p\right) = 2.3\,f\,(6.2 + 17.2) = 82.8\,f$$

$$C_w = 250\,f$$

$$\Rightarrow t_{pLH} = \frac{332.8\,(2.5)}{\frac{1}{2}\left(\frac{4}{4}\right)50\mu\,(4)^2} = \boxed{2.08\ ns}$$

e) Find the numerical value of the propagation delay t_p from the input to Inverter 1 to the output of Inverter 2. The drain-bulk capacitance can be neglected because of the large wire capacitance (Again, do take into account the gate capacitances of the driven gates). (6 points)

$$t_p = t_{p1} + t_{p2}$$

$$t_{p1} = \frac{C_L\left(V_{DD}/2\right)}{\frac{1}{2}\left(\frac{W}{L}\right)\mu_n C_{ox}\left(V_{DD}-V_{Tn}\right)^2}$$

$$C_L = C_G + C_w = C_{G,\,inv2} = C_{ox}\left(W_n L_n + W_p L_p\right)$$

$$= 2.3\ fF/\mu m^2\left(18.2 + 36.2\right) = 248\ fF$$

$$\Rightarrow t_{p1} = \frac{248\,f\,(2.5)}{50\mu\left(\frac{6}{4}\right)(4)^2} = \underline{.516\ ns}$$

$$t_{p2} = \frac{C_L\left(V_{DD}/2\right)}{\frac{1}{2}\left(\frac{W}{L}\right)\mu_n C_{ox}\left(V_{DD}-V_{Tn}\right)^2}$$

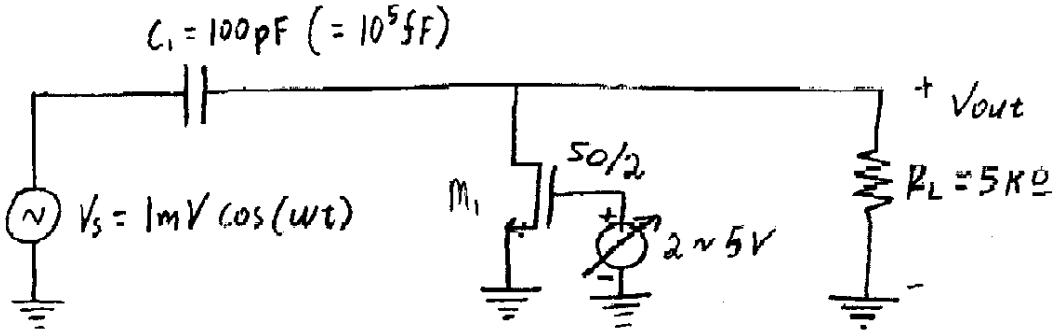
$$C_L = C_G + C_w = C_{G,\,nor} + 750\,f \qquad C_G = 2.3\left(16.2 + 4.2\right) = 92\,f$$

$$\Rightarrow C_L = 750 + 92 = 842\,f$$

$$\Rightarrow t_{p2} = \underline{.585\ ns} \qquad \Rightarrow t_p = t_{p1} + t_{p2} = .516 + .585 = \boxed{1.1\ ns}$$

Problem 4 of 4 (25 points)

Consider the following circuit. Note that this is NOT a common gate amplifier, since the transistor is only going to be operating in the *triode* region.



a) Note that this transistor is operating in the triode region and is playing the role of a variable resistor. Calculate the sheet resistance of the channel of this transistor, as a function of V_{GS}. Do this calculation for V_{GS} values of 2, 3, and 5V. (5 points)

USING THE HINT

TRIODE EQ. $I_D = \left(\frac{W}{L}\right)_1 \mu_n C_{ox}\left((V_{GS}-V_T)-\frac{V_{DS}}{2}\right)V_{DS} \quad (+\ \text{higher order } V_{DS})$

REMEMBER FROM LAB

$I_{D_{TRIODE}} \sim \left(\frac{W}{L}\right)_1 \mu_n C_{ox}(V_{GS}-V_T)V_{DS}$ FOR $V_{DS} \ll 1$

THEN $R_{M_1} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DS}}{\left(\frac{W}{L}\right)_1 \mu_n C_{ox}(V_{GS}-V_T)V_{DS}} = \frac{1}{\left(\frac{W}{L}\right)_1 \mu_n C_{ox}(V_{GS}-V_T)}$

BUT $R_{\square_{M_1}} \cdot \frac{L}{W} = R_{M_1} = \frac{1}{\mu_n C_{ox}(V_{GS}-V_T)}$

PLUGGING AND CHUGGING

V_{GS} (V)	$R_\square$ (Ohms/□)
2	$20 \cdot 10^3$
3	$10 \cdot 10^3$
5	$5 \cdot 10^3$

b) Given that the size of this transistor is 50/2, calculate the equivalent small signal channel resistance for its channel. (Hint: the small channel resistance in this case is NOT determined by the λ of the transistor!). (5 points)

$R = R_\square \frac{L}{W}$ (A LOT OF PEOPLE USED $R = R_\square \frac{W}{L}$ THIS IS A NO-NO)

$\frac{L}{W} = \frac{2}{50} \Rightarrow .04$

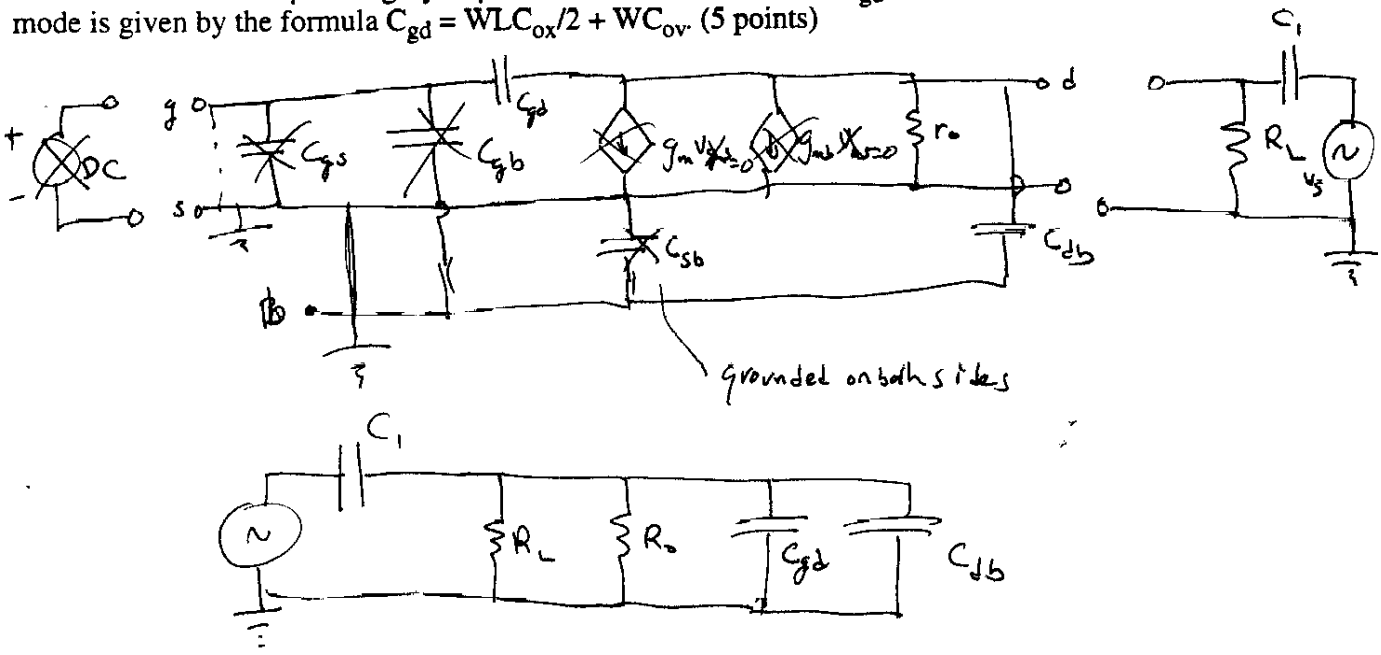
$R(2V) = 20 \cdot 10^3 \cdot .04 \Rightarrow 800\Omega$

$R(3V) = 10 \cdot 10^3 \cdot .04 \Rightarrow 400\Omega$

$R(5V) = 5 \cdot 10^3 \cdot .04 \Rightarrow 200\Omega$

V_{GS} (V)	$r_{channel}$ (Ohms)
2	800Ω
3	400Ω
5	200Ω

c) Write the small signal model and include and calculate the parasitic capacitances. Note that the size of the drain is 10μm long by 50μm wide. Also note that the C_{gd} for a transistor in a triode mode is given by the formula $C_{gd} = WLC_{ox}/2 + WC_{ov}$. (5 points)



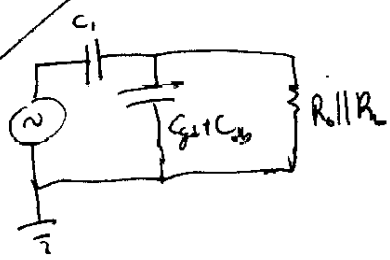
$C_{db} = C_{jn} \cdot W \cdot L_{diff} + C_{jsw} \cdot (W + 2 \cdot L_{diff})$

$= 85fF$

$C_{gd} = \frac{W \cdot L \, C_{ox}}{2} + W \cdot C_{ov}$

$= 18fF$

d) Calculate the first pole and first zero for this circuit for V_{GS} values of 2 and 5 volts and draw the two voltage transfer characteristics versus frequency for each value of V_{GS}. (Use the same graph for both plots, but make sure you mark each carefully.) (5 points)



pole at $\frac{1}{(R_0 \| R_L)(C_1)}$

$\frac{1}{(R_0 \| R_L)(C_{gs}+C_{db})}$

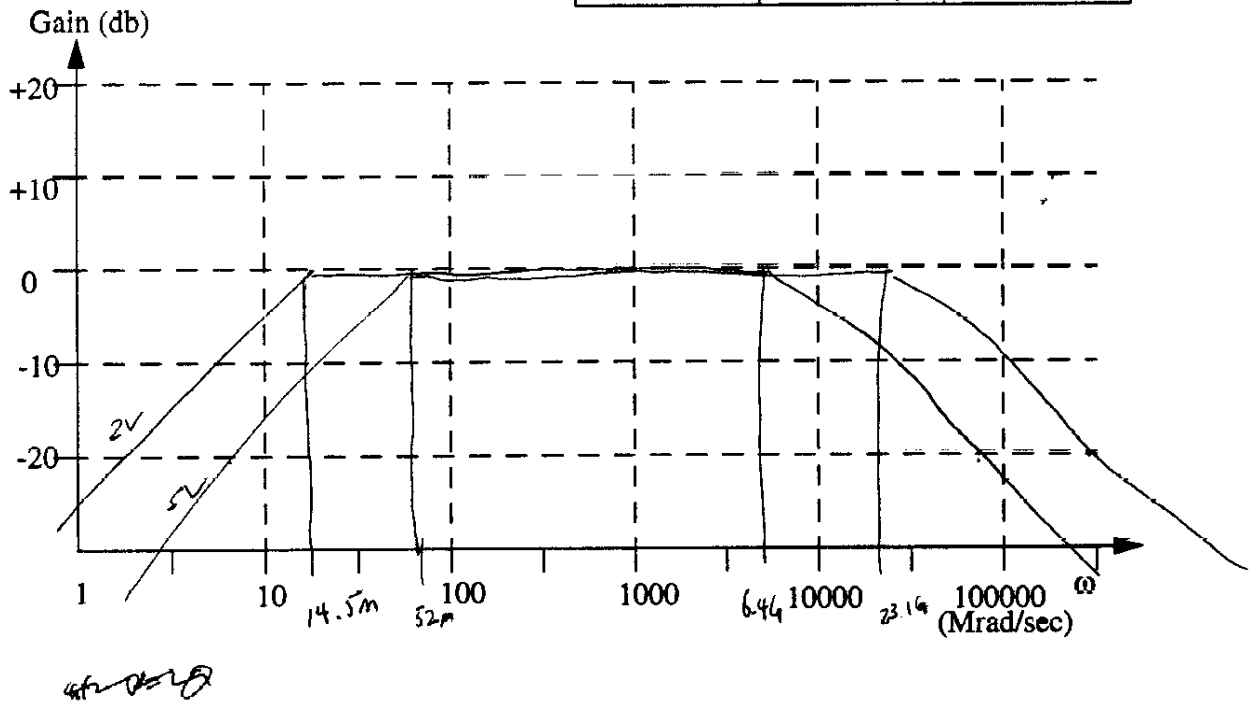
oops.
this circuit has a "zero" at zero frequency, and two poles, shown below.
its transfer function has the form:

$A \frac{jw}{(1+jwt_1)(1+jwt_2)}$

@ 2V
pole at $6.44\ G\frac{rad}{sec}$
$14.5\ M\frac{rad}{sec}$

@ 5V
pole at $23.1\ G\frac{rad}{sec}$
$52\ M\frac{rad}{sec}$

Parameter	Value when $V_{GS} = 2V$	Value when $V_{GS} = 5V$
first zero	0	0
first pole	$14.5\ M\frac{rad}{sec}$	$52\ M\frac{rad}{sec}$

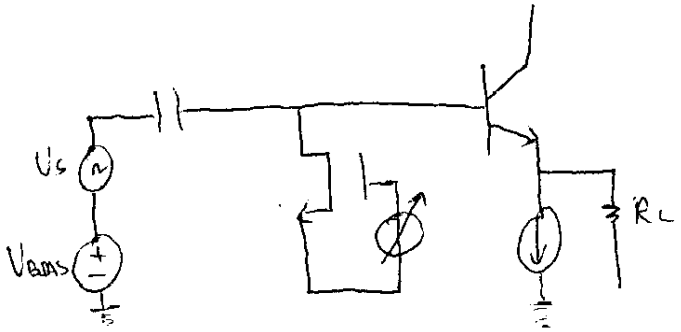


e) What amplifier stage would you consider adding between this filter and the load in order to make the frequency response of the entire circuit largely independent of the value of the load? (Note that you have to use a transistor type and an amplifier stage that will not limit the high frequency response of this filter). Draw the new circuit and explain your choice. (5 points)

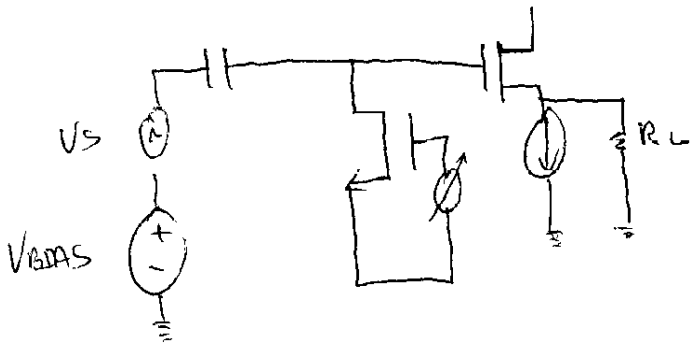
WE WANT:

1) BUFFERING, SPECIFICALLY VOLTAGE BUFFERRING

2) LARGE INPUT RESISTANCE, SMALL OUTPUT RESISTANCE AND NO MILLER EFFECT TO LIMIT BANDWIDTH



Common - Collector



Common - Drain

~ That's All Folks! ~