MOS Capacitor in Depletion

- Now we make $V_{GB} > V_{FB}$. Note that thermal equilibrium falls into this range of applied bias.

- Surface potential at oxide/silicon interface is now positive $\rightarrow$ n-type (slightly, $n_s = 10^{13} \text{ cm}^{-3}$).

The Threshold Voltage $V_{Tn}$

- Keep increasing $V_{GB} \rightarrow$ surface potential keeps increasing. At some point, the surface is n-type (i.e., we say that it is inverted).

- The gate-bulk potential at the onset of inversion is called the threshold voltage, $V_{Tn}$. To find the threshold voltage, we need to consider the electrostatics in depletion (no electrons at the surface at the onset of inversion) $\rightarrow$ with the surface potential equal to the opposite of the bulk potential:

$$\Phi_{x, max} = -\Phi_p$$
**Threshold Voltage Expression**

- We can solve for the threshold voltage:

\[
V_T - V_{FB} = V_{ox}' + V_{B, max}
\]

- The drop across the depletion region is

\[
V_{B, max} = \phi_s, max - \phi_p = -\phi_p - \phi_p = -2\phi_p
\]

- The drop across the oxide for \( V_{GB} = V_{Th} \) is

\[
V_{ox}' = E_{ox}' = \left( \frac{-Q_{B, max}}{E_{ox}} \right)_{ox} = -\frac{Q_{B, max}}{C_{ox}}
\]

- Substituting for the bulk charge (found from the potential drop across the depletion region, we find

\[
V_{Th} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \frac{2q\varepsilon_s N_a}{-2\phi_p}
\]

**The Inverted MOS Capacitor (\( V_{GB} > V_{Th} \))**

- We consider the surface potential as fixed ("pinned") at \( \phi_{s, max} = -2\phi_p \)

\[
\phi_{s, max} = -2\phi_p
\]

- Inversion charge \( Q_N \) at SiO\(_2\) - silicon surface balances extra + charge on gate as \( V_{GB} \) increases

\[
Q_N = -C_{ox}(V_{GB} - V_{Th})
\]
### Charge Storage in the MOS Structure

- Three regions of operation:
  - **Accumulation:** \( q_G = C_{ox} (v_{GB} - v_{FB}) \) ... parallel plate capacitor
  - **Depletion:** \( q_G = -q_B(v_{GB}) \), with the bulk (depletion) charge in the silicon being a nonlinear function of \( v_{GB} \)
  - **Inversion:** \( q_G = -q_N - q_{B,max} \), where \( q_{B,max} = q_B(v_{GB} = V_T) \) is the depletion charge at the onset of inversion and
- Sketch of the gate charge as a function of gate-bulk voltage:

![Gate Charge vs. Gate-Bulk Voltage](image)

### MOS Capacitance

- The capacitance of the MOS structure is defined as
  \[
  C = \frac{dq_G}{dv_{GB}}|_{V_{GB}}
  \]
- From sketch, determine the slope and plot as the capacitance:

![MOS Capacitance](image)
Physical Interpretation of MOS Capacitance

- **Accumulation**: parallel plate capacitor \( \rightarrow C = C_{ox} \)

- **Depletion**: increment in gate charge is mirrored at bottom of depletion region, so capacitance model is \( C_{ox} \) in series with the depletion region capacitance \( C_b \)

\[
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}
\]

\[
C_b = \frac{\varepsilon_s}{X_d}
\]

Note that \( X_d \) is a function of \( V_{GB} \)

\[
C = C_{ox} \parallel C_b
\]

- **Inversion**: bulk charge is no longer changing with \( V_{GB} \) \( \rightarrow \) an increment in gate charge is “mirrored” in the inversion layer under the gate.

The capacitance is therefore the same as in accumulation \( \rightarrow C = C_{ox} \)

MOS Field Effect Transistors
MOSFET Circuit Symbols

Two complementary devices (each with two symbols): both are very useful

p-substrate (n-type channel under gate oxide)
n-substrate (p-type channel under gate oxide)

Four electrical terminals: source (lowest potential for n-channel, highest for p-channel), drain, gate, and bulk.

Basic concept: inversion layer (called the channel) formed under gate between source and drain enables drift current