Common-Drain Amplifier

- Similar configuration to common collector.

![Common-Drain Amplifier Diagram]

Analysis: much the same as for CC amplifier -- if $V_{SB}$ isn’t zero, then the voltage gain is degraded from about 1 to 0.8-0.9
Common-Drain Two-Port Model

- Two-Port model:

If $V_{SB} = 0$, then the input resistance is $A_v = 1$ and $R_{out} = 1 / g_m$ (for hand analysis).

The CD amplifier is a reasonable voltage buffer, especially for large $(W/L)$ --> large $g_m$. 

![Diagram of common-drain two-port model]
Single-Stage Amplifier Configurations

- Two complementary versions exist for each amplifier type.
- CS/CE, CG/CB, and CD/CC have similar topologies (and properties)

<table>
<thead>
<tr>
<th>Amplifier Type</th>
<th>Transistor Type</th>
<th>NMOS</th>
<th>PMOS</th>
<th>npn</th>
<th>pnp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Source/ Common Emitter (CS/CE)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common Gate/ Common Base (CG/CB)</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Common Drain/ Common Collector (CD/CC)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
# Two-Port Parameters for Single-Stage Amplifiers

<table>
<thead>
<tr>
<th>Amplifier Type</th>
<th>Controlled Source</th>
<th>Input Resistance $R_{in}$</th>
<th>Output Resistance $R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Emitter</td>
<td>$G_m = g_m$</td>
<td>$r_\pi$</td>
<td>$r_o \parallel r_{oc}$</td>
</tr>
<tr>
<td>Common Emitter + $R_E$</td>
<td>$G_m = g_m / (1 + g_m R_E)$</td>
<td>$r_\pi \left(1 + g_m R_E \right)$</td>
<td>$r_{oc} \parallel [(1 + g_m R_E) r_o]$, for $r_\pi \gg R_E, R_S$</td>
</tr>
<tr>
<td>Common Source</td>
<td>$G_m = g_m$</td>
<td>infinity</td>
<td>$r_o \parallel r_{oc}$</td>
</tr>
<tr>
<td>Common Base</td>
<td>$A_i = -1$</td>
<td>$1 / g_m$</td>
<td>$r_{oc} \parallel [(1 + g_m (r_\pi \parallel R_S) ) r_o]$, for $g_m R_S \gg 1$</td>
</tr>
<tr>
<td>Common Gate</td>
<td>$A_i = -1$</td>
<td>$1 / g_m$, ($v_{sb} = 0$) -otherwise- $1 / (g_m + g_{mb})$</td>
<td>$r_{oc} \parallel [(1 + g_m R_S) r_o]$, ($v_{sb} = 0$) -otherwise- $r_{oc} \parallel [(1 + (g_m + g_{mb}) R_S) r_o]$ both for $g_m R_S \gg 1$</td>
</tr>
<tr>
<td>Common Collector</td>
<td>$A_v = 1$</td>
<td>$r_\pi + \beta_o (r_o \parallel r_{oc} \parallel R_L)$</td>
<td>$(1 / g_m) + R_S / \beta_o$</td>
</tr>
<tr>
<td>Common Drain</td>
<td>$A_v = 1$ if $v_{sb} = 0$, -otherwise- $g_m / (g_m + g_{mb})$</td>
<td>infinity</td>
<td>$1 / g_m$ if $v_{sb} = 0$, -otherwise- $1 / (g_m + g_{mb})$</td>
</tr>
</tbody>
</table>

Note: appropriate two-port model is used, depending on controlled source
Ultra-Simplified Two-Port Parameters

- $g_{mb} = 0$, common base has reasonable source resistance -> $R_S >> r_\pi$

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<thead>
<tr>
<th>Amplifier Type</th>
<th>Controlled Source</th>
<th>Input Resistance $R_i$</th>
<th>Output Resistance $R_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Emitter</td>
<td>$G_m = g_m$</td>
<td>$r_\pi$</td>
<td>$r_o \parallel r_{oc}$</td>
</tr>
<tr>
<td>Common Source</td>
<td>$G_m = g_m$</td>
<td>infinity</td>
<td>$r_o \parallel r_{oc}$</td>
</tr>
<tr>
<td>Common Base</td>
<td>$A_i = -1$</td>
<td>$1 / g_m$</td>
<td>$r_{oc} \parallel (\beta r_o)$</td>
</tr>
<tr>
<td>Common Gate</td>
<td>$A_i = -1$</td>
<td>$1 / g_m$</td>
<td>$r_{oc} \parallel [(1+g_m R_S) r_o]$</td>
</tr>
<tr>
<td>Common Collector</td>
<td>$A_v = 1$</td>
<td>$r_\pi + \beta (r_o \parallel r_{oc} \parallel R_L)$</td>
<td>$(1 / g_m) + R_S / \beta$</td>
</tr>
<tr>
<td>Common Drain</td>
<td>$A_v = 1$</td>
<td>infinity</td>
<td>$1 / g_m$</td>
</tr>
</tbody>
</table>

- this table is adequate for first-cut hand design
Multistage Amplifiers

- Single-stage transistor amplifiers are inadequate for meeting most design requirements for any of the four amplifier types (voltage, current, transconductance, and transresistance.)

- Therefore, we use more than one amplifying stage. The challenge is to gain insight into when to use which of the 12 single stages that are available in a modern BiCMOS process:

  - Bipolar Junction Transistor: CE, CB, CC -- in npn and pnp * versions
  - MOSFET: CS, CG, CD -- in n-channel and p-channel versions
  - * in many BiCMOS technologies, only the npn BJT is available

- How to design multi-stage amplifiers that satisfy the required performance goals?

* Two fundamental requirements:

1. Impedance matching:

   output resistance of stage $n$, $R_{out, n}$ and input resistance of stage $n + 1$, $R_{in, (n+1)}$, must be in the proper ratio

   $R_{in, (n+1)} / R_{out, n} \rightarrow \infty$ or $R_{in, (n+1)} / R_{out, n} \rightarrow 0$

   to avoid degrading the overall gain parameter for the amplifier

2. DC coupling:

   direct connection between stages --> interaction between biasing sources must be considered (later)
Cascaded Voltage Amplifier

- Want $R_{in} \to \infty$, $R_{out} \to 0$, with high voltage gain.

Try CS as first stage, followed by CS to get more gain ... use 2-port models

- solve for overall voltage gain ... higher, but $R_{out} = R_{out2}$ which is too large
Three-Stage Voltage Amplifier

- Fix output resistance problem by adding a common drain stage (voltage buffer)

- Output resistance is not that low ... few kΩ for a typical MOSFET and bias --> could pay an area penalty by making \((W/L)\) very large to fix.
Transconductance Amplifier

- Input resistance should be high; output resistance should also be high.
- Initial idea: use CS stages (they are "natural" transconductance amps).

\[
G_m = -g_m (r_{o1} || r_{oc1}) g_{m2} v_{in1}
\]

Overall, \( G_m = -g_m (r_{o1} || r_{oc1}) g_{m2} = A_{v1} g_m \ldots \) can be very large.

- Output resistance is only moderately large.
Improved Transconductance Amplifier

- Output resistance: boost using CB or CG stage

\[
\begin{align*}
\text{CS} - \text{CS} & \quad A_{v1}g_{m2}v_{in} \quad r_{oc2} \parallel r_{oc3} \\
\text{CG} & \quad -i_{in3} \quad g_{m3}r_{oc2} \parallel r_{oc3}
\end{align*}
\]

- high-resistance current sources are needed to avoid having \( r_{oc3} \) limit the resistance
Two-Stage Current Buffers

- since one CB stage boosted the output resistance substantially, why not add another one ...

- The base-emitter resistance of the 2nd stage BJT is $r_{\pi 2}$ which is much less than the 2nd stage source resistance = 1st stage output resistance

\[
R_{S2} = R_{out1} = \beta_{o1} r_{o1} || r_{oc1}
\]

- Therefore, the output resistance expression reduces to

\[
R_{out} \approx g_{m2} r_{o2} r_{\pi 2} || r_{oc2} = \beta_{o2} r_{o2} || r_{oc2}
\]

... no improvement over a single CB stage
Improved Current Buffer: CB/CG

- The addition of a common-gate stage results in further increases in the output resistance, making the current buffer closer to an ideal current source at the output port.

- The product of transconductance and output resistance $\frac{g_m}{r_o}$ can be on the order of 500 - 900 for a MOSFET --> $R_{out}$ is increased by over two orders of magnitude.

  Of course, the current supply for the CG stage has to have at least the same order of output resistance in order for it not to limit the overall $R_{out}$.

  Practical limit ... on the order of 100 MΩ