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Problem Set #5
Due Wednesday, September 30th, 1998

EECS105 **FALL 1998**

Default values: unless the problem states otherwise, use $\mu_n C_{ox} = 50\ \mu A/V^2$, $\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{Tn} = 1$ V, $V_{Tp} = -1$ V, $\lambda_n = 0$, $\lambda_p = 0$.

1. Take a look at the gorgeous circuit your TA painstakingly designed in Adobe Photoshop (it's on the next page). It's relatively common in modern circuit design.

   a. First we'll analyze the NMOS device. Here's a few important numbers for the calculation. The oxide thickness is 100 Angstroms for the whole device. The p-type doping is $N_a = 10^{17}$ cm^{-3}, while the source and drains are n^+ with $N_d >> 10^{17}$ cm^{-3}. Assume for the time being that V_{DS} and V_{GS} are 2 V. Finally $C_{OV} = .5$ fF/μm. Find these small signal capacitances: C_{gs}, C_{gd}, C_{sb}, and C_{db}. Draw a quick sketch of the small signal model with these capacitances included. You don't need to calculate g_m, g_{mb}, or r_0.

   b. Use SPICE to draw the IV characteristics of the NMOS transistor. HINT: use a circuit similar to the one in the textbook, Figure 4.3a. Your graph should be much like 4.3b (without the V_{DS} line). But make sure to use the correct dimensions!

   c. Sketch a schematic of the entire circuit, correctly labeling the PMOS and NMOS transistors (you don't need to draw their small signal models). What logic function does this circuit implement?

   d. Use SPICE to simulate the voltage transfer characteristics -- V_{out} vs. V_{in} -- of the circuit. Please turn in your *.cir file and a plot of V_{out} vs. V_{in} for $V_{in} = 0$ to 5 volts.

   e. (Extra-credit) Maybe you noticed that the two transistors are sized differently. Can you come up with a theory on why the designer would have done this?

2. More MOSFET excitement. You are looking to analyze an NMOS transistor with the following characteristics: W/L = 20 μm/3 μm, $V_{GS} = 2$ V, $V_{DS} = 3.5$ V, $V_{BS} = 0$ V.

   a. Find the DC drain current I_D.

   b. Now a small signal $v_{gs}(t) = 20$ mV cos $(2\pi*1000*t)$ is added in series with V_{GS}. What is the small-signal drain current $i_d(t)$? You can ignore g_{mb} and r_0 for this calculation (assume they are zero).

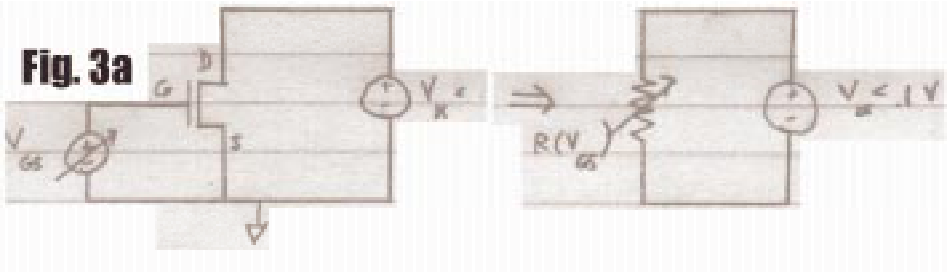
   c. Plot the total current $i_D(t)$ vs. time (for t=0 to 3 ms) from the answers in part (a) and (b).

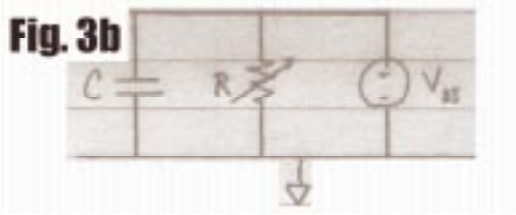
3. Occasionally analog circuits require large, voltage-controlled resistors. Design a NMOS transistor with a resistance of 1 MΩ for V_{GS} = 1.5 V (see Figure 3a). Your process parameters: the minimum feature size is 2 µm, the substrate doping $N_a = 10^{17}$ cm^{-3}, C_{ox} = 1.42 $fF/\mu m^2$, C_{OV} = .5 fF/µm, and the poly gate is n^+.

   a. How would you size the NMOS, i.e. what should its width and length be?

   b. Find the capacitance between the channel and the gate, and between the gate and the drain? What is the total capacitance due to these two caps? HINT: I know we haven't given you a formula for the first capacitance, but try to visualize what area it represents capacitance over…it's simple when you picture the transistor!

   c. Now think of the transistor as a low-pass RC filter (see Figure 3b). Find the break (-3 dB) frequency using the resistance and the two capacitance's solved for above . HINT: For those who haven't taken EECS 120: the break frequency for this device will occur at w (omega) = $2\pi f = RC^{-1}$. This should help **a lot**!





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Please return your homework in 558 Cory Hall, to Cheryl Craigwell (cmc@eecs, 642-1237, fax 642-2739), by 11am of the due date. Late homeworks will not be graded.