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Problem Set #7
Due Wednesday, October 14th, 1998

EECS105 **FALL 1998**

Default values to use on this problem set:

$V_{Tn} = -V_{Tp} = 1$ V, $V_{DD} = 5$ V, $\lambda_N = \lambda_P = 0$ V^{-1},
C_j (NMOS) = .3 fF/μm^2, C_j (PMOS) = .5 fF/μm^2
C_{jsw} (NMOS) = .8 fF/μm, C_{jsw} (PMOS) = .135 fF/μm
Oxide = $SiO_2 = 3.9\varepsilon_o$
$L_{diffn} = L_{diffp} = 6$ μm

Gate Oxide Thickness	*CVD Oxide Thickness*	*Thermal Oxide Thickness*
.1 μm	.5 μm	.7 μm

1. Just what you needed: another unclear circuit layout sketch. The circuit is simply two inverters in series, each made of four parallel NMOS and PMOS transistors, doped with $N_a = N_d = 10^{16}$ cm^{-3} -- we are going to analyze the first inverter's characteristics using the second inverter essentially as a load device. The thick black line denotes the active area of each device. This time we are going to find the capacitances needed to calculate the propagation delay of the gate and the energy dissipated by it.

   a. Please calculate all the relevant capacitances that affect the propagation delay of the first inverter: C_P, C_G, C_W and C_L. For the wire capacitance calculation, just use the metal1 layer that connects the output of the first inverter to the second.

   b. Next, use the capacitance you just calculated to derive t_{PLH}, t_{PHL}, and t_P for the FIRST inverter only.

   c. Draw a small signal model of both inverters, solving for all the relevant values: g_{mn}, g_{mp}, r_{on}, r_{op}. Now calculate the important voltage transfer characteristics: V_{OH}, V_{OL}, V_{IL}, V_{IH}, A_V, V_M and draw the VTC for the first inverter. To keep the calculations simple, you can assume $\lambda_N = \lambda_P = 0$ for all calculations except for r_{on}, r_{op}. For output resistance calculations, use $\lambda_N = 19.6$ V^{-1} and $\lambda_P = 5.4$ V^{-1}.

d. Let's take a look at the dynamic energy consumption of the first inverter.

Transition: Low to High	*Energy Amount*	*Is the energy Stored/Dissipated/Not Applicable?*
Power supply? C_L? NMOS? PMOS? *Transition: High to Low* Power supply? C_L? NMOS? PMOS?		

e. Say this is a gate on the Pentium II processor, which has approximately $8 * 10^6$ devices and runs at 400 Mhz. How much power would this chip burn? The PII is actually built on a .25 μm process and runs internally at 1.8 V. Redo the calculation for power, dividing C_L by 8 and using the new V_{DD}. Does this still seem high? If so, can you explain what might make this calculation give an unrealistically high estimate for power consumption?

2. You are given a standard CMOS inverter with $(W/L)_n = 3/1.5$ and $(W/L)_p = 6/1.5$, $\mu_n C_{ox} = 50$ $\mu A/V^2$, $\mu_p C_{ox} = 25$ $\mu A/V^2$, and $C_{ox} = 2.3$ $fF/\mu m^2$. Ignore wire capacitance. What is the maximum fan-out possible (i.e. how many external gates can this device drive?) that keeps $t_{PHL} < 600$ ps with:

   a. $V_{DD} = 5$ V?

   b. $V_{DD} = 2.5$ V?

3. A measure of the efficiency of a chip is its power-delay product, which is defined as the energy consumed by a gate per switching even (i.e 1 to 0 or 0 to 1). The formula for PDP is simply $P_D t_p$, where P_D is the dynamic power dissipation and t_p is the propagation delay. Plot this product as a function of V_{DD} fro $2.5 V < V_{DD} < 5$ V. For the calculations, use a CMOS inverter with $(W/L)_n = 3/1.5$ and $(W/L)_p = 6/1.5$, $\mu_n C_{ox} = 50$ $\mu A/V^2$ and $\mu_p C_{ox} = 25$ $\mu A/V^2$ driving three (3) identical inverters. Assume the clock frequency is 50 MHz.

4. A little logic question to make you think outside the box, as they say. Please draw a CMOS implementation of the function x (OUT) = $\overline{(A + BCD)}$. If you struggle with this, take a look at the book's implementations of NAND and NOR gates in CMOS. Writing out the truth table may help as well.