University of California
College of Engineering
Department of Electrical Engineering and Computer Sciences

Problem Set #8
Due Wednesday, Oct. 21, 1998

EECS105 **FALL, 1998**

Please refer to page 319 and page 442 for additional parameters when necessary.

1. In the static CMOS technology it is more area-efficient to design with NAND gates rather than NOR gates. Using the specifications of Design Example 5.8, design a 2-input NOR gate which meets the same performance requirements. Please follow each of the questions to guide your design. Use the same MOS device data as in Design Example 5.8. The minimum width of the CMOS technology is 1.5 μm.
   (a) Draw a circuit schematic for the 2-input NOR gate and label the transistors, input and output terminals. What input switching corresponds to the worst case propagation delay? From that deduce the relationship between the size of the p-channel transistors and size of the n-channel transistors, in order to have $t_{PHL} = t_{PLH}$.
   (b) Find the constraint on the load capacitance for which the delay requirements are satisfied? (Hint: express the constraint in terms of W_n.) Find the sizes for the transistors.
   (c) Sketch the three possible voltage transfer characteristics and label the important break points (Hint: find the V_M for each transfer curve).
   (d) Verify your result with SPICE simulation. Plot the three transfer characteristics. Iterate your design if necessary. (But, you don't have to repeat part (c).)
   (e) What is the additional area required for the NOR gate over the NAND gate design?

2. Please refer to Figure P5.21 in Page 327. Assume $\mu_n C_{ox}$ = 50μA/V^2, $\mu_p C_{ox}$ = 25 μA/V^2. Given the n-channel 2-input NOR gate,
   (a) Choose *W/L* of M_1, M_2 and M_E such that $t_{PHL} = t_{PLH}$. Assume *W/L* of M_1, M_2 and M_E are the same.
   (b) Calculate t_p for this gate assuming C_L = 0.4 pF. Neglect C_{DB} and C_{WIRE}.
   (c) What is the total device area $\Sigma(W(L+2L_{diff}))$?
   (d) What is the total area for a static CMOS 2-imput NOR gate which satisfies the same requirement as in (a)?

3. Do *Exercise* 7.5 on page 444
4. Do *Problem* 7.18 on page 454

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***Please post your questions on our newsgroup*:** ucb.class.ee105
Please return your homework in 558 Cory Hall, to Cheryl Craigwell (cmc@eecs, 642-1237, fax 642-2739), or in class by 11:10am of the due date. Late homeworks will not be graded.