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College of Engineering
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Problem Set #9
Due Wednesday, October 28th, 1998

EECS105

FALL 1998

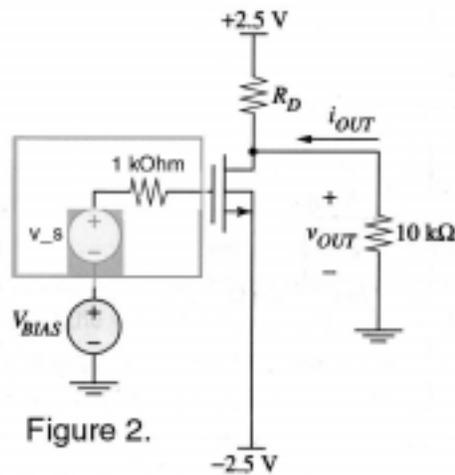
Default values to use on this problem set:

$$V_{Tn} = -V_{Tp} = 1 \text{ V}, V_{DD} = 5 \text{ V}, \mu_n C_{OX} = 50 \mu\text{A}/\text{V}^2, \mu_p C_{OX} = 25 \mu\text{A}/\text{V}^2$$

1. Time for some fun with a seemingly simple gate, the XOR.
 - a. Draw the truth table for an XOR, i.e. $X = A \oplus B$.
 - b. Design a static CMOS implementation of the XOR function using the minimum amount of NAND, and NOR gates. How many transistors does it take?
 - c. Design a dynamic CMOS implementation of the XOR. To avoid a nasty problem called charge sharing (which occurs during evaluate, when the charge originally stored entirely on the load capacitance distributes itself over devices in the PUN/PDN), alternate between ϕ_n and ϕ_p blocks. Don't get confused with the terminology; ϕ_n simply means the dynamic logic is built with a pull down network and ϕ_p means a pull up network. Make sure that the networks are evaluating at the same time (how can you ensure this?)! How many transistors does this dynamic implementation take?
 - d. Design the XOR using pass transistor logic. Again, how transistors gates does it take? You can use inverted signals, but make sure to add the devices in these inverters to your total gate count.
 - e. Finally, adapt your answer for part (d) to use transmission gates. How many transistors does this add to your solution from part (d)? Why would you want to use transmission gates?
 - f. Now you've seen 4 implementations of an XOR. Taking into account area, speed, noise margins and power consumption concerns, which seems like the best design solution? You don't have to solve for everything, just give a qualitative answer.
2. Take a look at Figure 2. It's a MOSFET amplifier. These will be your friends for the next few weeks – sad but true. Use the device characteristics given above, as well as the interesting fact that this transistor's $(W/L) = 30/3$. Other values: $\lambda_N = 0$.
 - a. What type of amplifier is this (common gate, common source, or common drain)?
 - b. How should we bias this amplifier (i.e., what are the values of R_D and V_{BIAS}) so that $I_D =$

500 μA when $V_{\text{OUT}} = 0 \text{ V}$?

- What are the two-port parameters R_{in} and R_{out} ?
- Draw the small-signal model of this amplifier.
- Calculate the unloaded voltage gain A_V and transconductance G_M , as well as the overall (loaded) voltage gain.



3. Let's examine another amplifier, this time the one in Figure 3. $\lambda_N = .02 \text{ V}^{-1}$, $W/L = 10/5$, and $r_{\text{oc}} = r_o$.

- Again, which type of amplifier is this?
- What should the bias current I_{BIAS} be so that $V_{\text{OUT}} = 0 \text{ V}$ when $I_{\text{SUP}} = 100 \mu\text{A}$?
- Derive the two-port parameters R_{in} and R_{out} .
- What is the unloaded current gain A_I and the unloaded transresistance R_M ?
- What is the loaded current gain and transresistance?

