EECS 105 – Microelectronic Devices and Circuits

Spring 2001, Prof. A. R. Neureuther
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Final Exam, May 14, 2001 (3 hours)

Print Your Name: SOLUTIONS

Sign Your Name: _____

Unless specified assume that r_{oc} is infinite and ignore the body effect. Use the following parameters for L = 2 μm MOS and Bipolar devices.

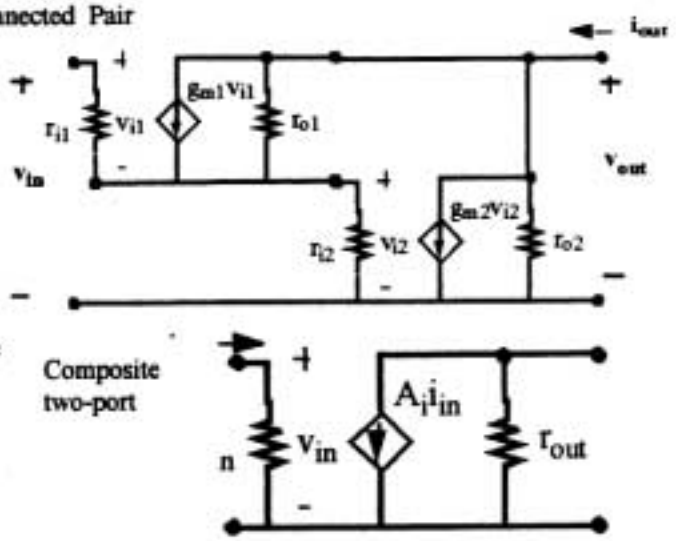
NMOS	PMOS
$\mu_n C_{ox}$=50μA/V^2	$\mu_p C_{ox}$=25μA/V^2
V_{TOn}=1.0V	V_{TOp}=-1.0V
γ_n=0.6V$^{1/2}$	γ_p=0.6V$^{1/2}$
λ_n=(0.1/L)V^{-1} L in μm	λ_p=(0.1/L)V^{-1} L in μm
ϕ_p=-0.42 (N_a=10^{17}/cm^3)	ϕ_n=0.42 (N_d=10^{17}/cm^3)
C_{ox}= 2.3 fF/μm^2	C_{ox}= 2.3 fF/μm^2
C_{OV}=0.2fF/μm	C_{OV}=0.2fF/μm

NPN	PNP
β=100	β=50
$V_{CE\text{-}SAT}$=0.1V	$V_{EC\text{-}SAT}$=0.1V
V_{BE}=0.7V	V_{EB}=0.7V
V_A=20V	V_A=25V
C_{jC} = 20 fF C_{jE} = 30 fF	τ_F = 50 ps

Problem	Possible	Score
I	35	
II	35	
III	30	
IV	35	
V	25	
VI	40	
Total	200	

I (35 Points) Circuit Analysis and Circuit Intuition

The interconnected pair of devices is to be replaced by a composite current amplifier two-port model. Each device has its own individual transconductance two-port model. The parameters of the composite two-port are to be expressed only in terms of the parameters for the individual device two-ports, namely, r_{i1}, g_{m1}, r_{o1}, r_{i2}, g_{m2}, and r_{o2} and the load R_L.



a) (12 Points) Find the current gain A_i of the composite two-port model and **give a short intuitive explanation of the result**.

SHORT OUTPUT

$v_{i1} = i_{IN} r_{i1}$

$v_{i2} = (i_{IN} r_{i1} g_{m1} + i_{IN})(r_{o1} \| r_{i2})$

$i_{OUT} = g_{m1} v_{i1} - \frac{v_{i2}}{r_{o1}} + g_{m2} v_{i2}$

$A_i = \frac{i_{OUT}}{i_{IN}} = g_{m1} r_{i1} + \left(g_{m2} - \frac{1}{r_{o1}}\right)(r_{i1} g_{m1} + 1)(r_{o1} \| r_{i2})$

$A_i \simeq (r_{i1} g_{m1})(g_{m2})(r_{o1} \| r_{i2})$

PRODUCT OF CURRENT GAIN OF BOTH STAGES WITH INTERNAL SHORT LOSS FACTOR

b) (10 Points) Specify a complete set of equations for finding R_{IN} for the composite two-port model.

ATTACH R_L
APPLY i_{in}

$i_{in} + g_{m1} r_{i1} i_{in} + \frac{v_{out} - v_a}{r_{o1}} - \frac{v_a}{r_{i2}} = 0$ (1)

$-g_{m1} r_{i1} i_{in} + \frac{(v_a - v_o)}{r_{o1}} - g_{m2} v_a - \frac{v_o}{r_{o2}} - \frac{v_o}{R_L} = 0$ (2)

(3) $v_{in} = i_{TEST} r_{i1} + v_a$
SOLVE FOR v_a

NOTE: $v_{i1} = r_{i1} i_{in}$ $v_{i2} = v_a$

SOLVE (2) FOR $v_o = f(v_a, i_{in})$

SUB INTO (1) $\Rightarrow v_a = (\,) i_{in}$

THEN SUBSTITUTE IN (3).

c) (13 Points) Assume r_{o2} and R_L are infinite. Solve for R_{IN} and **give a short intuitive explanation of the result**. Do not do 30 minutes of algebra with the above equations. Use the fact that the current from the second device completes its circuit by flowing through the parallel combination of g_{m1} and r_{o1}.

USING THE HINT (OR JUST NAME v_o)

$g_{m1} v_{i1} + \frac{v_o - v_a}{r_{o1}} = -g_{m2} v_a$

NOW THE ENTIRE NODE v_a

$i_{IN} - g_{m2} v_a - \frac{v_a}{r_{i2}} = 0$

$v_a = \frac{i_{IN}}{g_{m2} + \frac{1}{r_{i2}}}$

$v_{IN} = i_{IN} r_{i1} + v_a$

$\frac{v_{IN}}{i_{IN}} = R_{IN} = r_{i1} + \frac{1}{\left(g_{m2} + \frac{1}{r_{i2}}\right)}$

$r_{IN} = r_{i1} + \left(\frac{1}{g_{m2}} \| \frac{1}{r_{i2}}\right)$

THE CURRENT SOURCE g_{m2} CREATES A CURRENT PROPORTIONAL TO THE VOLTAGE ACROSS IT AND BECOMES A RESISTOR $\frac{1}{g_{m2}}$ IN PARALLEL WITH r_{i2}.

II. (35 Points) Device Physics

a) (12 Points) Suppose an npn transistor is to be redesigned to exactly double β and exactly cut τ_F in half. If only N_A and w_B are to be adjusted, find their new values in terms of the old values. Neglect the effect of doping on mobility.

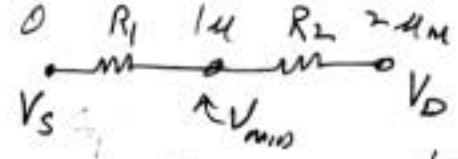
$$\tau_F \propto \frac{()}{W_B^2} \Rightarrow W_B' = \frac{W_B}{\sqrt{2}}$$

$$\beta \propto \frac{N_E D_{nB}/W_B}{N_A D_{nB}/W_B} \propto \frac{1}{N_A W_B} \Rightarrow N_A' = \frac{N_A}{\sqrt{2}}$$

b) (8 Points) Complete the following sentence. "The law of the junction is used in developing the relationship for current versus voltage for a diode to relate ... "

the density of minority carriers entering the opposite sides of the junction to the voltage on the junction."

c) (15 Points) Suppose an error in fabrication created an L = 2 μm device with a threshold voltage of 1V from the source to the1 μm midpoint, and a threshold voltage of 2V from this midpoint to the drain. Model this device as two resistors in series. Determine the gate voltage at which this device will begin to conduct and estimate the fraction of drain voltage that will appear at the midpoint of the channel when the gate voltage is 3V, the drain voltage is very small and the source is grounded.



$$V_{MID} = V_S + (V_D - V_S)\frac{R_1}{R_1 + R_2}$$

$G \propto$ # carriers $\propto (V_{GS} - V_T)$

$G_1 = ()(3-1) = ()2$

$G_2 = ()(3-2) = ()1$

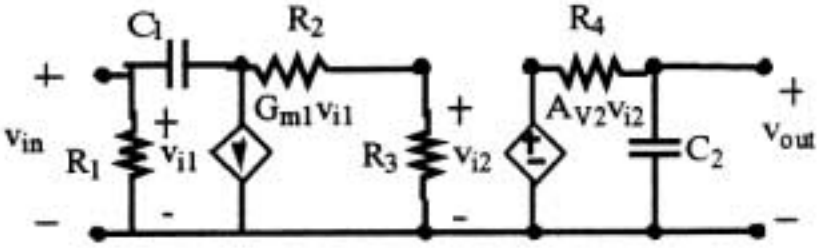
$R_1 = ()0.5 \quad R_2 = 01$

$$V_{MID} = \frac{1}{3} V_D$$

$V_{MID} = 1/3$ of drain voltage

III. (30 Points) Frequency Response

$G_{m1} = 1$ mS
$A_{V2} = 100$
$R_1 = 1$ kΩ
$R_2 = 20$ kΩ
$R_3 = 10$ kΩ
$R_4 = 5$ kΩ
$C_1 = 10$ fF
$C_2 = 100$ pF



a) (16 Points) Use the Miller approximation followed by the open-circuit time-constant method to find numerical values for the gain and ω_{3db} for the voltage transfer function v_{OUT}/v_{IN}.

$$\frac{v_{OUT}}{v_{IN}} = -G_{m1}(R_2+R_3)\frac{R_3}{(R_2+R_3)}(-A_{v_2}) = -(1mS)(10k\Omega)(+100) = -1000$$

C_1 sees $1+G_m(R_2+R_3) = 1+1mS(20K+10K) = 31$

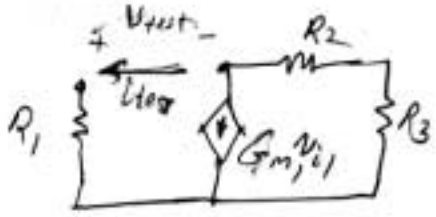
$$\Sigma\tau = C_1(1+G_m(R_2+R_3))R_1 + C_2R_4$$
$$= 10fF(31)(1k\Omega) + (100fF)(5k\Omega)$$
$$= 310ps + 500ps = 810ps$$

$\omega_{-3db} = 1.2$ krad/s
GAIN BW $= 1.2 \times 10^{12}$

b) (14 Points) If the Miller approximation were not used and a complete Bode plot were made, will the value found for ω_{3db} be the same, higher or lower than that found above? Answer and then explain by using a more rigorous and yet simple algebraic analysis to find the true algebraic expression for ω_{3db} of this circuit.

ω_{-3db} WILL BE LOWER

FIND R_{eq_1}



$\Sigma\tau$ INCREASES BY
$C_1(R_2+R_3) = (10fF)(30k)$
$= 300ps$

$\Sigma\tau = 1110ps$

$\omega_{-3} = 9.0 \times 10^8$

Apply i_{test}

SOURCE CURRENT GOES INTO TEST SOURCE

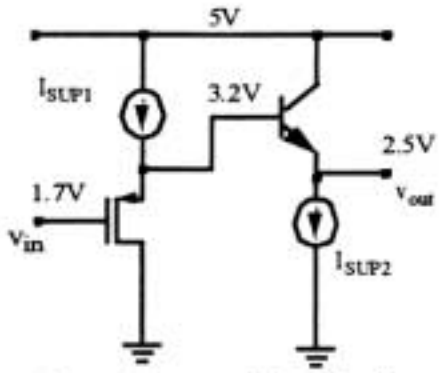
$$v_{test} = v_+ - v_-$$
$$= i_{test}R_1 - (-G_{m1}i_{test}R_1 - i_{test})(R_2+R_3)$$

$$\frac{v_{test}}{i_{test}} = R_{eq_1} = R_1 + G_{m1}R_1(R_2+R_3) + (R_2+R_3)$$

↑ NEW TERM

IV. (35 Points) Sources and Biasing

In this circuit the MOS device has a current supply of 20 μA and the bipolar device has a current supply of 60 μA.



a) (9 Points) Find the (W/L) of the PMOS device to accept I_{SUP1}. Assume the D.C. value of V_{IN} is 1.7V and neglect r_O of both the devices and the supplies. Also neglect the current between the stages.

FOR PMOS USE ABSOLUTE VALUES

$$I = \frac{1}{2}\left(\frac{W}{L}\right)_p \mu_p C_{ox} \left(|V_{GS} - V_{Tp}|^2\right)$$

$$\left(\frac{W}{L}\right)_p = \frac{2I}{\mu_p C_{ox} (|V_{GS} - V_{Tp}|^2)}$$

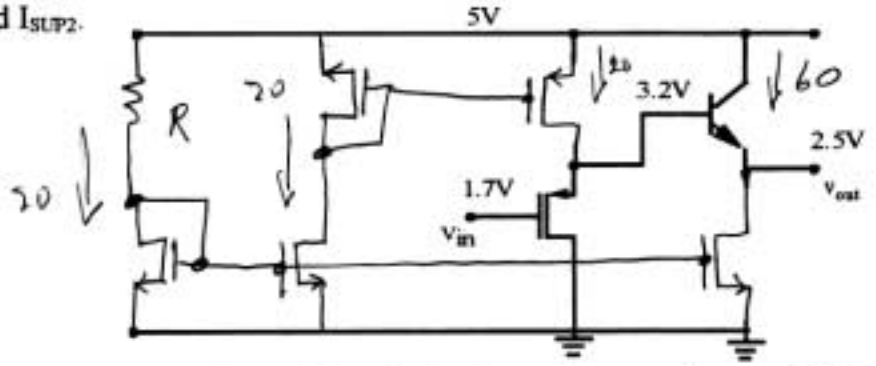
$V_{GS} = 1.7 - 3.2 = -1.5V$

$V_{TP} = -1$

$V_{GS} - V_{TP} = -1.5 - (-1) = -0.5$

$$= \frac{2(20u)}{25u(0.5)^2} = 6.4$$

b) (9 Points) Sketch additional MOS transistors and a resistor-based current reference to replace I_{SUP1} and I_{SUP2}.



c) (17 Points) Choose the resistor value and size the devices to be as small as possible and still provide the correct supply currents while allowing the circuit to swing from 0.8V to 4.0V for a 5V supply.

PMOS IN MOS START + 0.7 V_{BE} DROP LIMITS $V_{HIGH} = 1V$

$\Rightarrow V_{PMOS} = 0.3V$

PMOS ITSELF LIMITS V_{OUT} LOW AS $V_{SG} = 1.6V$

AND $V_{G\,MIN} = 0 \Rightarrow V_{S\,MIN} = 1.5V \Rightarrow V_{OUT} = 1.6V - V_{BE} = 0.8V$

PMOS DROP 0.3V TO NOT SATURATE $\Rightarrow V_G = 1.3V$

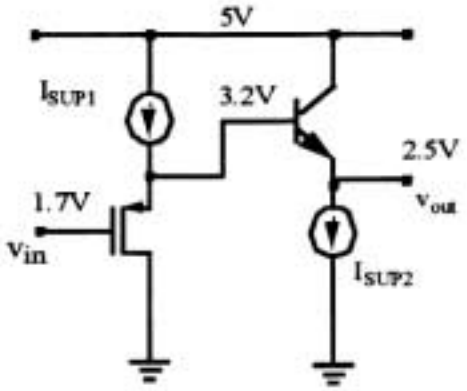
$$\left(\frac{W}{L}\right)_{P_{20uA}} = \frac{(2)(20uA)}{25uA/V^2 (1.3-1)^2} = 17.7$$

NMOS CAN GO UP TO 0.8V $\Rightarrow V_G = 1.8V$ AND STILL NOT SATURATE

$$\left(\frac{W}{L}\right)_{N_{20}} = \frac{(2)(20uA)}{50uA/V^2 (1.8-1)^2} = 1.25 \qquad \left(\frac{W}{L}\right)_{N=60uA} = 3(1.25) = 3.75$$

V. (25 Points) Small-Signal Performance

In this circuit the MOS device has a current supply of 20 μA and the bipolar device has a current supply of 60 μA. Assume $(W/L)_{PMOS} = 4$.



a) (13 Points) Use the two-port models for Bipolar/MOS single stages to estimate R_{IN}, R_{OUT} and v_{OUT}/v_{IN}.

$R_{IN} = \infty$

$g_{m_B} = \frac{I_C}{V_{th}} = \frac{60\mu A}{.025_{MV}} = 2.4mS \quad \frac{1}{g_{m_B}} = 417_{ohms}$

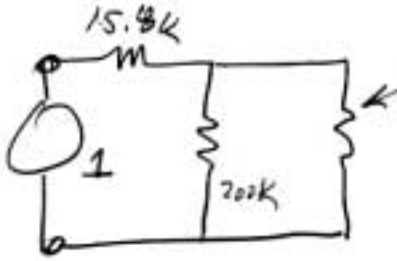
$\beta = 100$

$R_{o_{CC}} = \frac{1}{g_{m_B}} + \frac{R_S}{\beta_o} \rightarrow = 417_{ohms} + \frac{15.8k}{100} = 575_{ohms}$

$R_S = R_{o_{CD}} = \frac{1}{g_{m_{MOS}}}$

$g_{m_{MOS}} = \sqrt{2\left(\frac{W}{L}\right)\mu_p C_{ox} I_D} = \sqrt{(2)(4)\left(25\frac{\mu A}{V^2}\right)(20\mu A)} = 63.2\mu S \quad \frac{1}{g_{m_{MOS}}} = 15.8k$

b) (12 Points) What is the voltage loss between the MOS and bipolar stages due to the non-ideal nature of both the current source and the bipolar transistor. Assume $r_{oc1} = r_{oc2} = 200k\Omega$ and that the output is open circuited.



$r_\pi + \beta_o(r_o \| r_{oc})$

$r_o = \frac{V_{AB}}{I_C} = \frac{20}{60\mu A} = 333k\Omega$

$r_{oc} = 200k\Omega$

$(r_o \| r_{oc}) = 125k\Omega \xleftarrow{\text{WITH } \beta} \Rightarrow 12.5M\Omega$

$r_\pi = \frac{V_{th}}{I_B} = \beta\frac{V_{th}}{I_C} = \frac{(100)(.025V)}{60\mu A} = 41.7k$

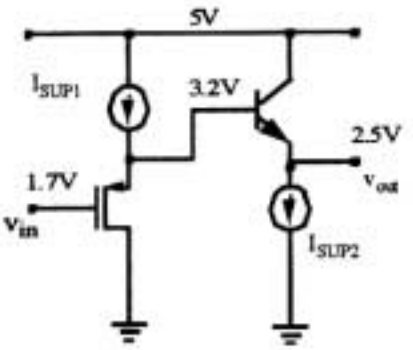
$\Rightarrow 12.5M\Omega$ so can neglect

$\frac{v_{out}}{v_{source}} = \frac{200k}{15.8k + 200k}$

$= 0.927$

VI. (40 Points) Frequency Response and Design

In this circuit the MOS device has a current supply of 20 μA and the bipolar device has a current supply of 60 μA. A source is added with resistance 300kΩ. A load is added that consists of 1 meter of cat-5 cable that has a capacitance of 1 pF/cm. Assume $r_{OC1} = r_{OC2} =$ 200kΩ and that $(W/L)_{PMOS} = 4$.



a) (12 Points) Make a simple argument as to why the capacitive effects between the stages will not likely limit the overall frequency response. (There are two aspects to this argument).

LOW IMPEDANCE C_{DPMOS} HAS LOW $r_{out} = \frac{1}{g_{mp}} \approx 25k\Omega$

NO CC HAS GAIN NEAR UNITY $\Rightarrow C_{IN\,TO\,OUT} \simeq 0$

MILLER EFFECT.

b) (12 Points) What is ω_{-3db} for the overall voltage gain when the both the source and load are attached?

$C_{gs} = \frac{2}{3} WL C_{ox} + W C_{ov} = \frac{2}{3}(9.2)\,2.3\,fF/\mu m^2 + 8\mu m(0.2fF)/\mu m = 26.1fF$

$24.5fF + 1.6fF$

$R_{IN} C_{gs} = 300k\Omega \cdot 26.1fF = 7.84ns$

$R_{OUT} C_{OUT} = (575)(100pF) = 57.5ns$

$65.3ns \Rightarrow \omega_{-3db} = 1.5 \times 10^7$

c) (8 Points) Could this circuit be redesigned with the same topology and device technology to increase ω_{-3db} significantly? Explain by identifying any major points of engineering leverage. Assess their potential improvement (1.2X, 1.5X, 2.0X, etc.) and give their down side.

A FACTOR OF ABOUT 5→8 COULD BE ATTAINED

BY INCREASING I_{SUP2} TO REDUCE R_{OUT} AND ← PROPORTIONAL $\frac{1}{I_{SUP2}}$

I_{SUP1} TO REDUCE $\frac{r_{o1}}{\beta}$ IN THE OUTPUT. ← PROPORTIONAL TO $\frac{1}{\sqrt{I_{SUP1}}}$

DOWNSIDE BURNS POWER $\propto (I_{SUP2} + I_{SUP1})$

EVENTUALLY $R_{IN} C_{GS}$ DOMINATES.

d) (10 Points) Could fabrication of the devices in this circuit in a more modern BiCMOS technology (with shorter gate length, higher β, and smaller junction areas) increase ω_{-3db} significantly? Assume the topology and biasing remains the same. Explain by identifying any major points of engineering leverage. Assess their potential (1.2X, 1.5X, 2.0X, etc.) and give their down side.

VERY LIMITED BENEFIT OF AT MOST 20%.

SMALLER L WILL REDUCE $R_{IN} C_{GS}$ BUT

THIS IS ONLY ½ OF THE DELAY.

DOWNSIDE - WAFER COST.