Lecture 7, January 2, 2001

EECS 105 Microelectronics Devices and Circuits, Spring 2001
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Topics:
W: Capacitance of pn junction;

Reading: HS 3.3-3.6. Light on math of the 2 sided model (3.4.2).
Example: pn Prototype

Equal area for charge neutrality

\[ E_{\text{MAX}} = qN_{\text{ax}}x_p/\varepsilon_{\text{si}} = qN_{\text{d}}x_n/\varepsilon_{\text{si}} \]

Parabolic dependence of \( x_n \) and \( x_p \) on potential \( \phi_B - V_D \)

\[ \phi_B = \phi_n - \phi_p = V_{th} \ln \left( \frac{N_d}{n_i} \right) - V_{th} \ln \left( \frac{N_a}{n_i} \right) \]
pn Junction: No Bias

\[
\phi_B = \phi_n - \phi_p = V_{th} \ln \left( \frac{N_d}{n_i} \right) - V_{th} \ln \left( \frac{N_a}{n_i} \right)
\]
**pn Junction: Reverse Bias**

$V_D$ is the applied reverse voltage
Effect of Applied Reverse Voltage

Analog Integrated Circuits
Effect of Applied Reverse Voltage

Effect of Applied Reverse Voltage

Effect of Applied Reverse Voltage

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Effect of Applied Reverse Voltage
Algebraic Results: pn-Prototype

\[ \phi_B = \phi_n - \phi_p = V_{th} \ln\left( \frac{N_d}{n_i} \right) - V_{th} \ln\left( \frac{N_a}{n_i} \right) \]

\[ x_{po} = \sqrt{\frac{2\varepsilon_s (\phi_B - V_D)}{qN_a}} \left( \frac{N_d}{N_a + N_d} \right) \quad x_{no} = \sqrt{\frac{2\varepsilon_s (\phi_B - V_D)}{qN_d}} \left( \frac{N_a}{N_a + N_d} \right) \]

\( V_D \) is the applied reverse voltage

\[ x_{do} = x_{no} + x_{po} \quad E_0 = -\frac{qN_d x_{no}}{\varepsilon_s} = \frac{qN_a x_{po}}{\varepsilon_s} \]

One sided approximation adequate when \( N_a \) and \( N_d \) differ by more than an order of magnitude.
Physical Example

\[ N_a = 10^{16} \text{cm}^{-3} \quad N_d = 10^{18} \text{cm}^{-3} \quad V_D = -15 \text{V} \]

\[
\phi_n = V_{th} \ln \left( \frac{N_d}{n_i} \right) = 0.026 \ln \left( \frac{10^{18}}{1.4 \times 10^{10}} \right) = 470 \text{mV} \\
\phi_p = -V_{th} \ln \left( \frac{N_a}{n_i} \right) = -0.026 \ln \left( \frac{10^{16}}{1.4 \times 10^{10}} \right) = -350 \text{mV} \\
\phi_B = \phi_n - \phi_p = 470 \text{mV} - (-350 \text{mV}) = 720 \text{mV}
\]

\[
x_{po} = \sqrt{\frac{2 \varepsilon_s \phi_B}{qN_a}} = \sqrt{\frac{2(11.7)(8.85 \times 10^{-14} \text{Fcm}^{-1})(0.72)}{1.6 \times 10^{-19} \text{C}}} = 0.305 \mu \text{m}
\]

\[
x_p(V_D) = \sqrt{\frac{2 \varepsilon_s (\phi_B - V_D)}{qN_a}} = x_{po} \sqrt{1 - \frac{V_D}{\phi_B}} = 0.305 \sqrt{1 - \frac{-15 \text{V}}{0.72 \text{V}}} = 1.43 \mu \text{m}
\]
Definition of Depletion Capacitance

Capacitance is a small signal concept

\[ C_j = \frac{q_j}{v_d} \]

Capacitance can be viewed as charge separated by distance

\[ C''_j = \frac{\varepsilon_{si}}{x_d} \]

\[ q_J = Q_J + q_j \]
Graphical Interpretation

\[ V_D \quad v_D = V_D + v_d \]

\[ q_j = Q_J + q_J \]

slope = \( C_j(V_D) \)
Visualization of Junction Cap.

Capacitance can be viewed as charge separated by distance.

$$C''_j = \frac{\varepsilon_{\text{si}}}{X_d}$$
Spice Computer Simulation Model

\[ C_j = \frac{C_{JO}}{\left(1 - \frac{V_D}{V_J}\right)^M} \]

- \( C_{JO} = C_{jo} \) the zero bias (equilibrium) capacitance
- \( V_J = \phi_B \) the built-in barrier voltage
- \( M = \) the grading coefficient of the junction (0.3 to 0.7)

Caution: Capacitance per unit area or per unit length of layout perimeter are often used.
Capacitance as a Resistor Parasitic

Layout gives a distributed RC Circuit! The capacitance and delay are voltage dependent.
Depletion Capacitance of an IC Resistor

\[ C_{jo} = \frac{\varepsilon_{si}}{x_{do}} \]
\[ = \frac{(11.7)(8.85 \times 10^{14} \text{F/cm}^{-1})}{0.635 \text{ um}} \]
\[ = 16.3 \times 10^{-9} \text{ F/cm}^2 \]

\[ AR = LW + 2(3W)^2 = 16.25 \times 10^{-6} \text{cm}^2 \]

\[ C_R = C_{jo}A_R \]
\[ = (16.3 \times 10^{-9} \text{ F/cm}^2)(16.25 \times 10^{-6} \text{cm}^2) \]
\[ = 26.5 \text{fF} \]

\[ R = 64.2k\Omega \quad RC = 1.7\text{ns} \]