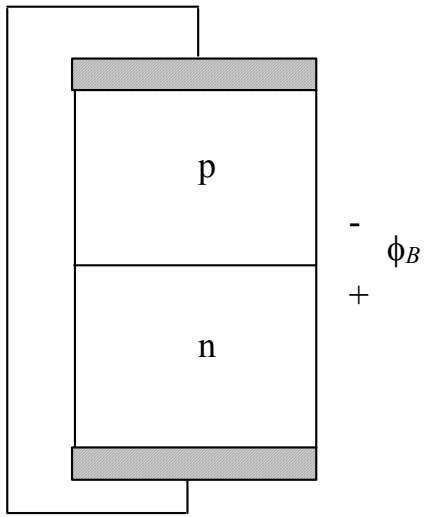
Lecture 10

- Last time:
  - IC resistors (finish)
  - IC capacitors (metal-metal + start pn junction)
- Today :
  - pn junction: reverse bias
  - *Q-V* plots → linearization to get C_j

Voltages in Thermal Equilibrium

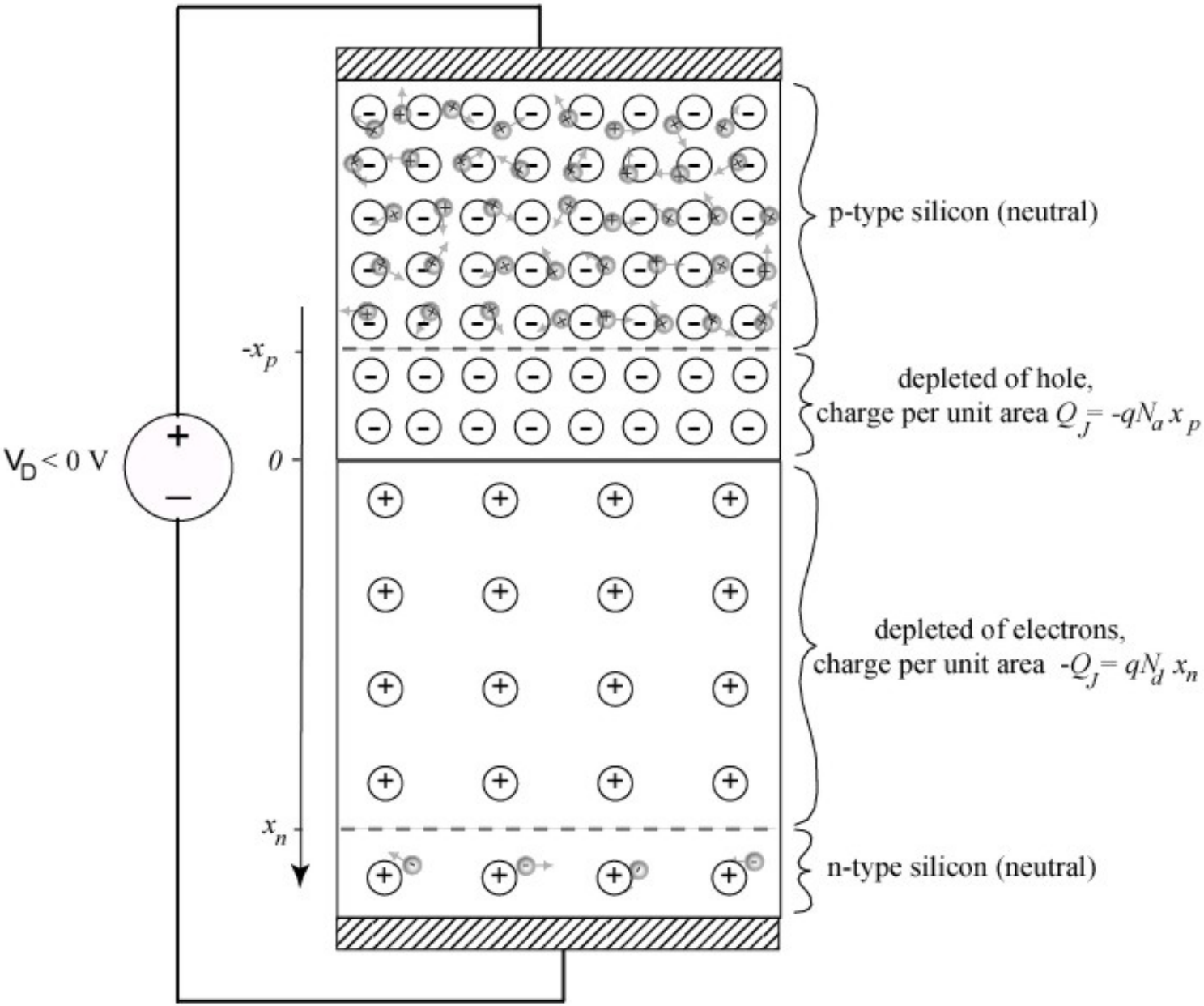


KVL: where are the missing voltage drops?

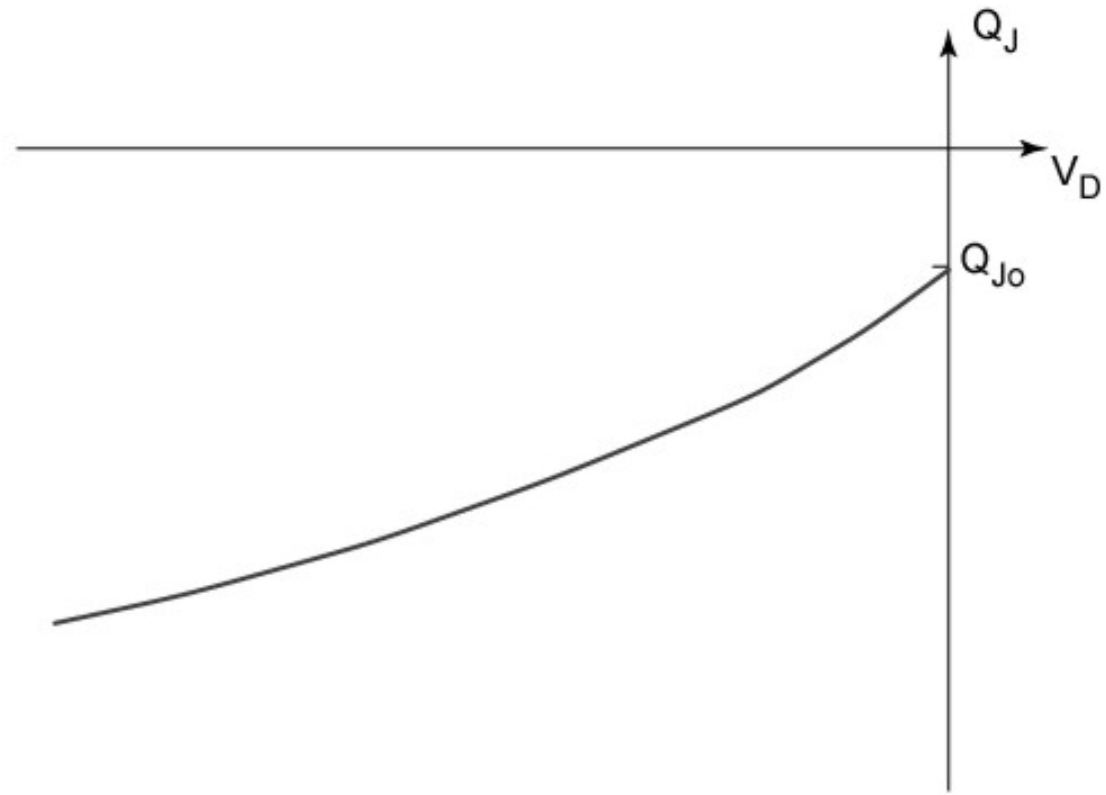
Reverse Applied Bias ($V_D < 0$ V)

- Polarity increases charge stored in junction
  → increases barrier between p and n regions

- Current is negligible (due to high barrier)


p-type silicon (neutral)
depleted of hole,
charge per unit area $Q_J = -qN_a x_p$
depleted of electrons,
charge per unit area $-Q_J = qN_d x_n$
n-type silicon (neutral)
$-x_p$
0
x_n
$V_D < 0$ V
+
–

Qualitative Charge-Voltage Plot



Why isn't the plot linear?

Quantitative Charge-Voltage Plot

Approximations are needed … see EE 130

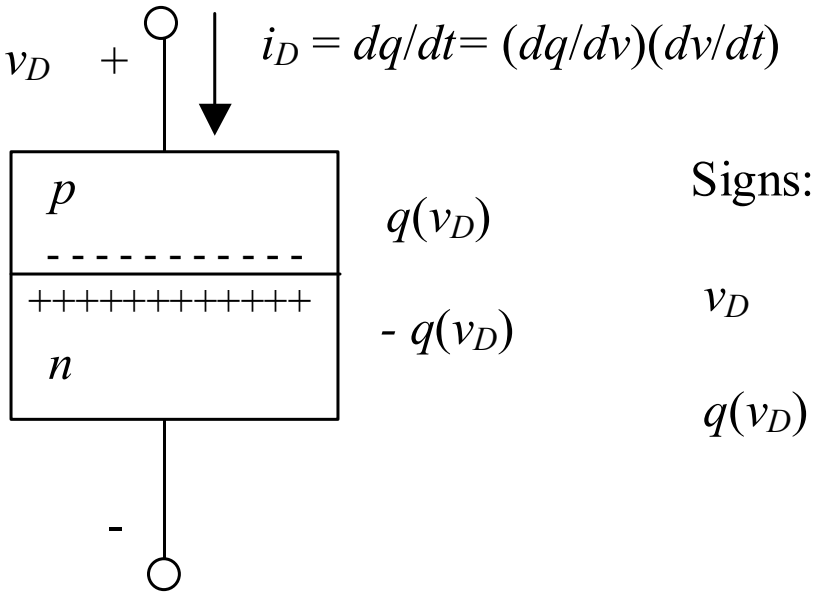
Lengthy derivation in HS 3.4-3.5 (not assigned)

Result: $$Q_J = Q_{Jo}\sqrt{1 - V_D / \phi_B}$$

Built-in voltage ϕ_B

Charge Storage in pn Junction

- Circuit element:

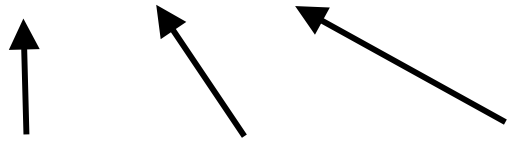


- Can't handle non-linearity in KCL, KVL

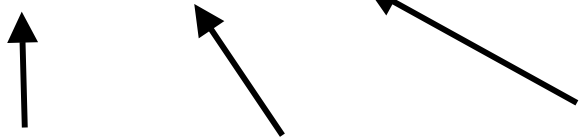
Linearizing the Charge Storage

- Symbol conventions

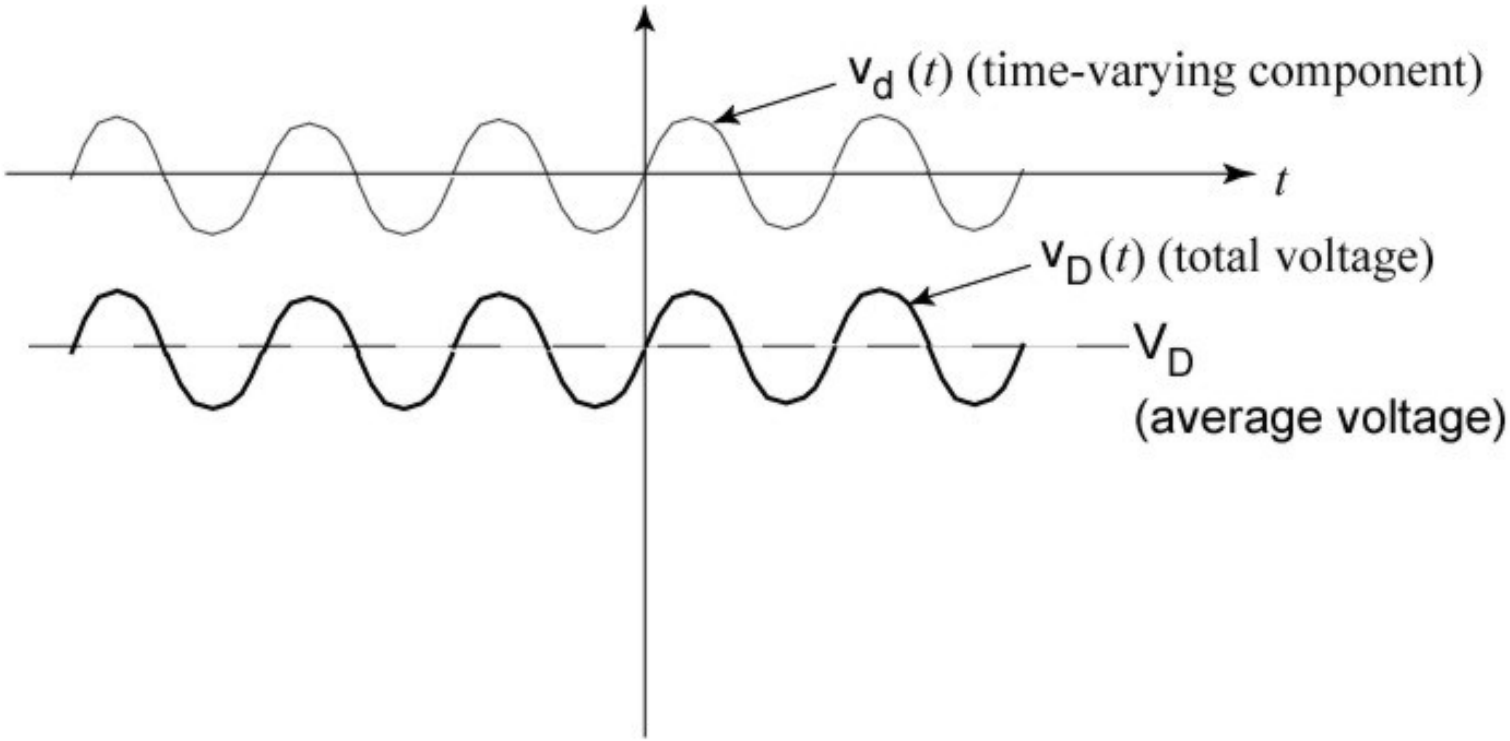
$$q_J = Q_J + q_j$$



$$v_D = V_D + v_d$$



Diode Voltage $v_D(t)$



Incremental Charge q_j